

Compal Confidential

BIUS4/S5 & CIUY0/Y1

DIS M/B Schematics Document

Intel KabyLake U Processor with DDR4

AMD R16M-M1-30/R16M-M2-50

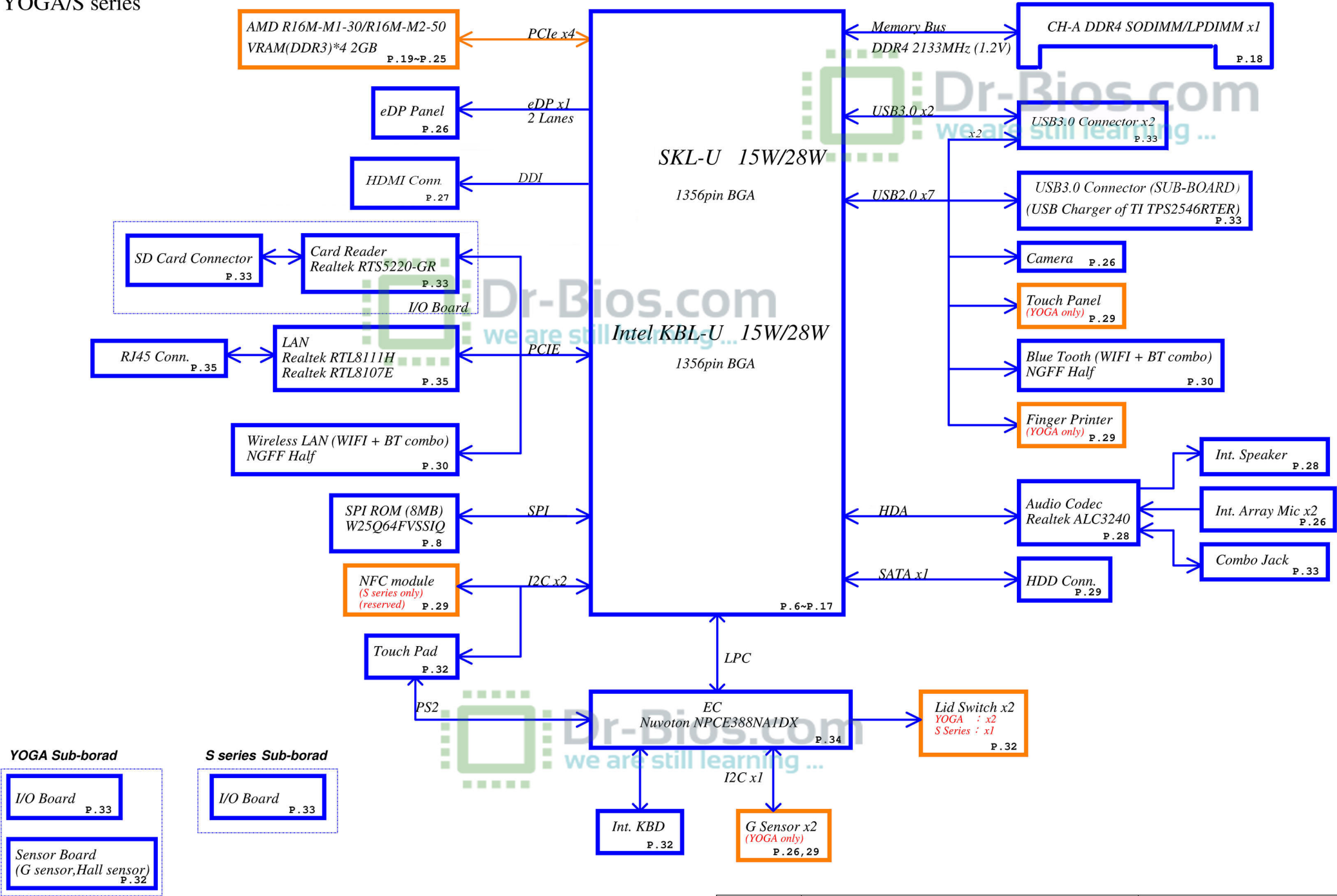
2016-06-27

LA-E221P

REV : 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/04/07	Deciphered Date	2017/02/16	Title	Cover Page
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YOGA/S series



Voltage Rails

State	power plane	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.35VS +1.0VS_VCCOPC +VCC_CORE +VGA_CORE +VCC GFXCORE_AXG +1.8VS +0.75VS +1.0VALW
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

BOM Structure Table

Item	BOM Structure
LAN 10/100 Transformer	100@
LAN Giga Transformer	GIGA@
For Giga LAN Chip	8111H@
For 10/100 LAN Chip	8107E@
For DIS	DIS@
For UMA	UMA@
For GPU M1 Chip	M1@
For GPU M2 Chip	M2@
For NFC Option	NFC@
For Thermal Chip	EX_THM@
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For K/B 15 inch NUM LED	15_NUM@
For VARM X76	GM_X76@
For Hynix Memory	H2G@
For Samsung Memory	S2G@
For Micron Memory	M2G@
For EMI	EMI@
For ESD	ESD@
No EMI	@EMI@
No ESD	@ESD@
No RF	@RF@
For RF	RF@
Connector	ME@
For Test Point	TP@
For 2+3E power	23E@
For YOGA series only	YOGA@
For 14 inch only	S14@
For 15 inch only	S15@
For 15 inch UMA EXTRA	UMA_EXTRA@
For SKL CPU Type	6500U@
	6200U@
	6100U@
	4405U@
For KBL CPU Type	KS@
	JW@

CV194_RF@ only for DIS

USB 2.0 Port Table

Port	External USB Port
1	Touch panel (for YOGA only)
2	USB2/3 MB(JUSB1)
3	USB2/3 MB(JUSB2)
4	USB2 IO Board(Charger)
5	Camera
6	
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	
2	USB2/3 MB(JUSB1)
3	USB2/3 MB(JUSB2)
4	
5	
6	

SATA Port Table

Port	
0	HDD
1	

PCIe Port Table

Port	Lane	
1	1	GPU
2	2	
3	3	
4	4	
5		LAN
6		
7		NGFF WLAN+BT
8		
9		
10		

EC SM Bus1 address EC SM Bus2 address EC SM Bus4 address ME SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	0001 011x 16h	NCT7718W	1001 100x 98h	BMA250E	0001 100x 18h	NFC	0010 1000 28h

PCH SM Bus address

GPU SM Bus address

Device	Address	Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h	Internal thermal sensor	1001 111x 9Eh

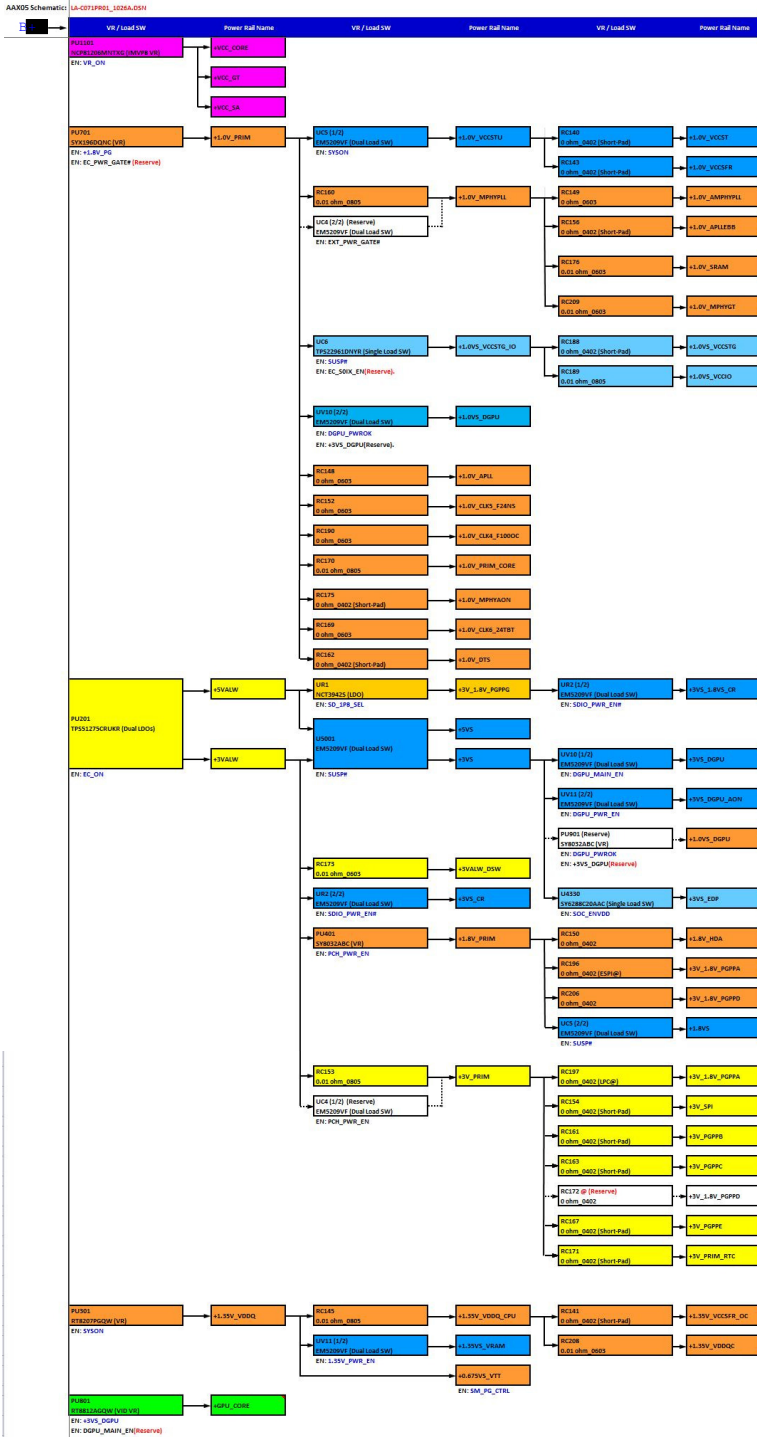
SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU	CRT RT2168	NFC	TP	PCH	G-SENSOR
SMB_EC_CK1	NECP388	✗	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW	+3VALW	+19V_VIN										
SMB_EC_CK2	NECP388	✓	✗	✗	✓	✗	✓	✗	✗	✗	✓	✗	
SMB_EC_DA2	+3VS	+3VGS			+3VS		+3VS				+3VS		
SMB_EC_CK4	NECP388	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✓	
SMB_EC_DA4	+3VALW											+3VS	
PCH_SMBCLK	PCH	✗	✗	✗	✗	✓	✗	✗	✗	✗	✓	✗	✗
PCH_SMBDATA	+3VALW					+3VS					+3VS		
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✗	✗
SML0DATA	+3VALW									+3VS			
SML1CLK	PCH	✗	✗	✗	✓	✗	✗	✓	✗	✗	✗	✗	✗
SML1DATA	+3VALW				+3VS			+3VS					

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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BIVS3/ VE3 -PowerMap_SKL-U22_DDR3L_Volume_NON CS]

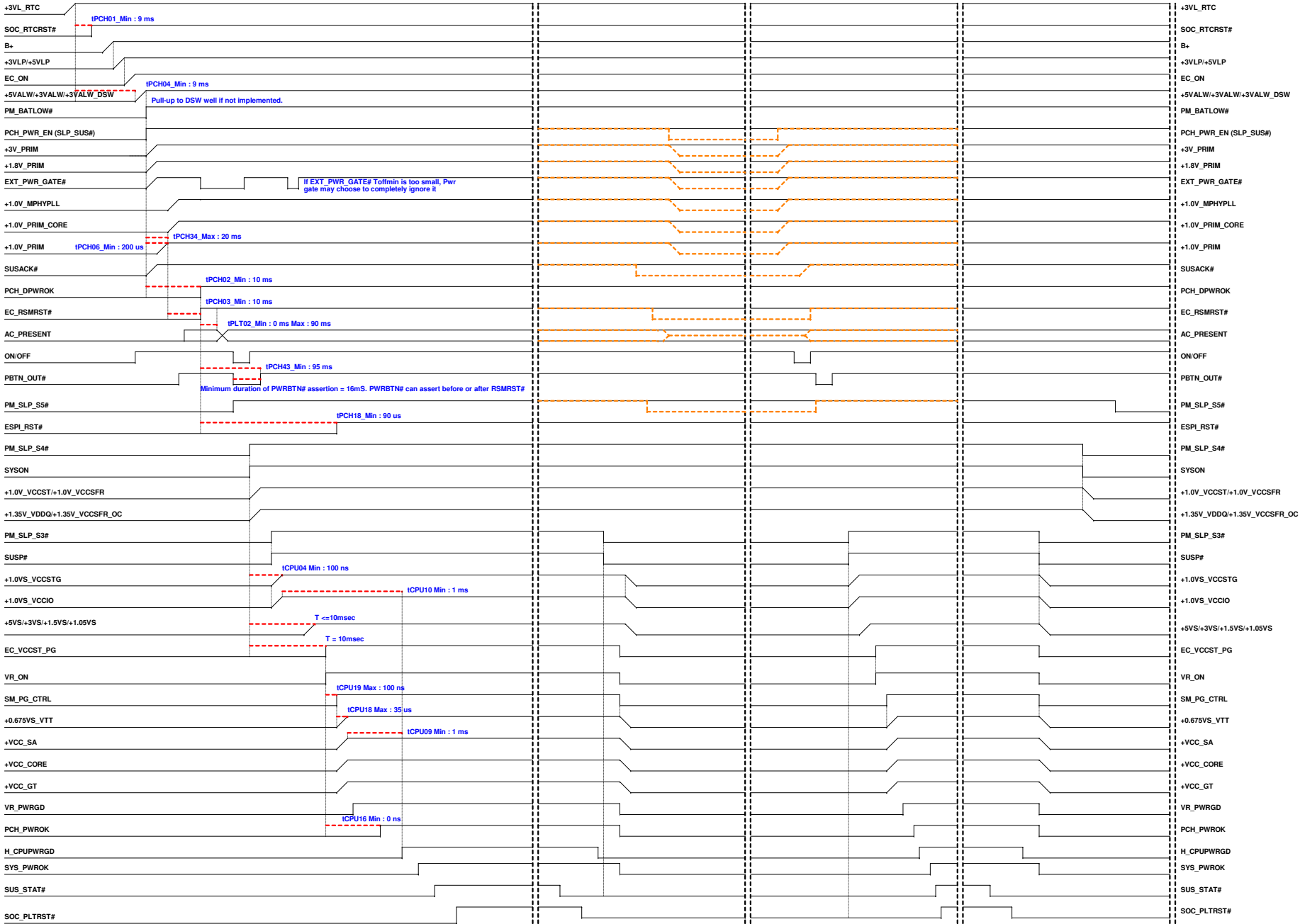
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G3→S0

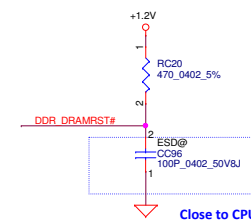
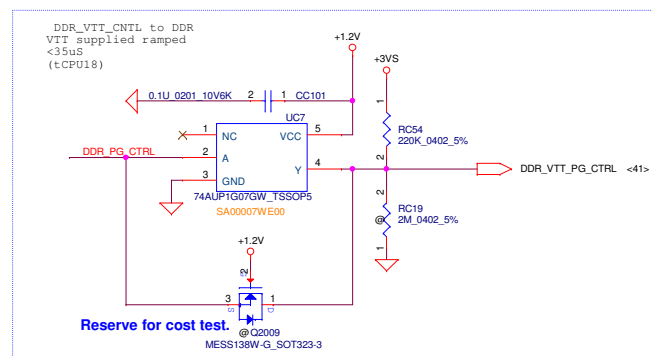
S0→S3/DS3

S0/DS3→S0

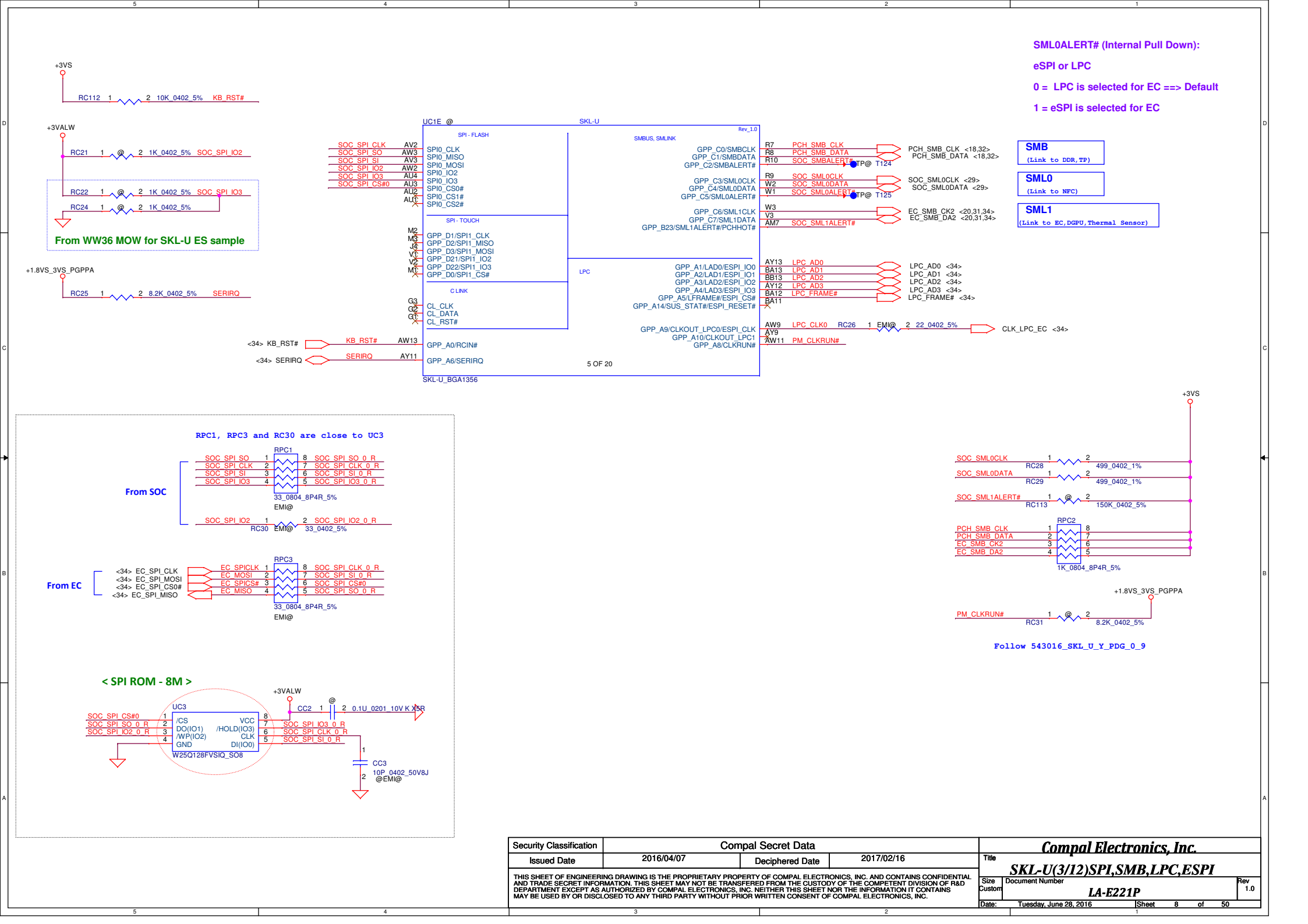
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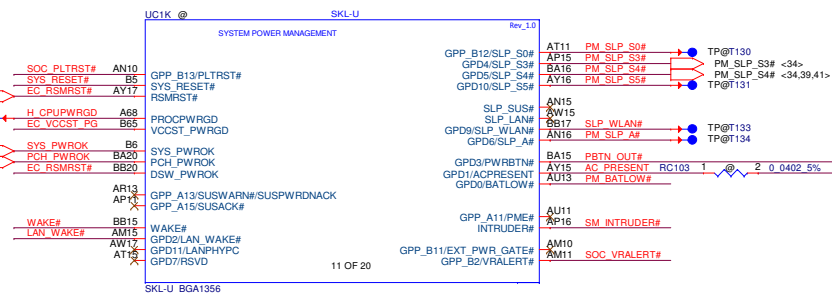
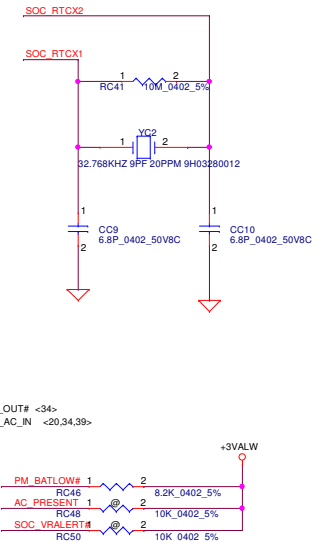


Interleaved Memory



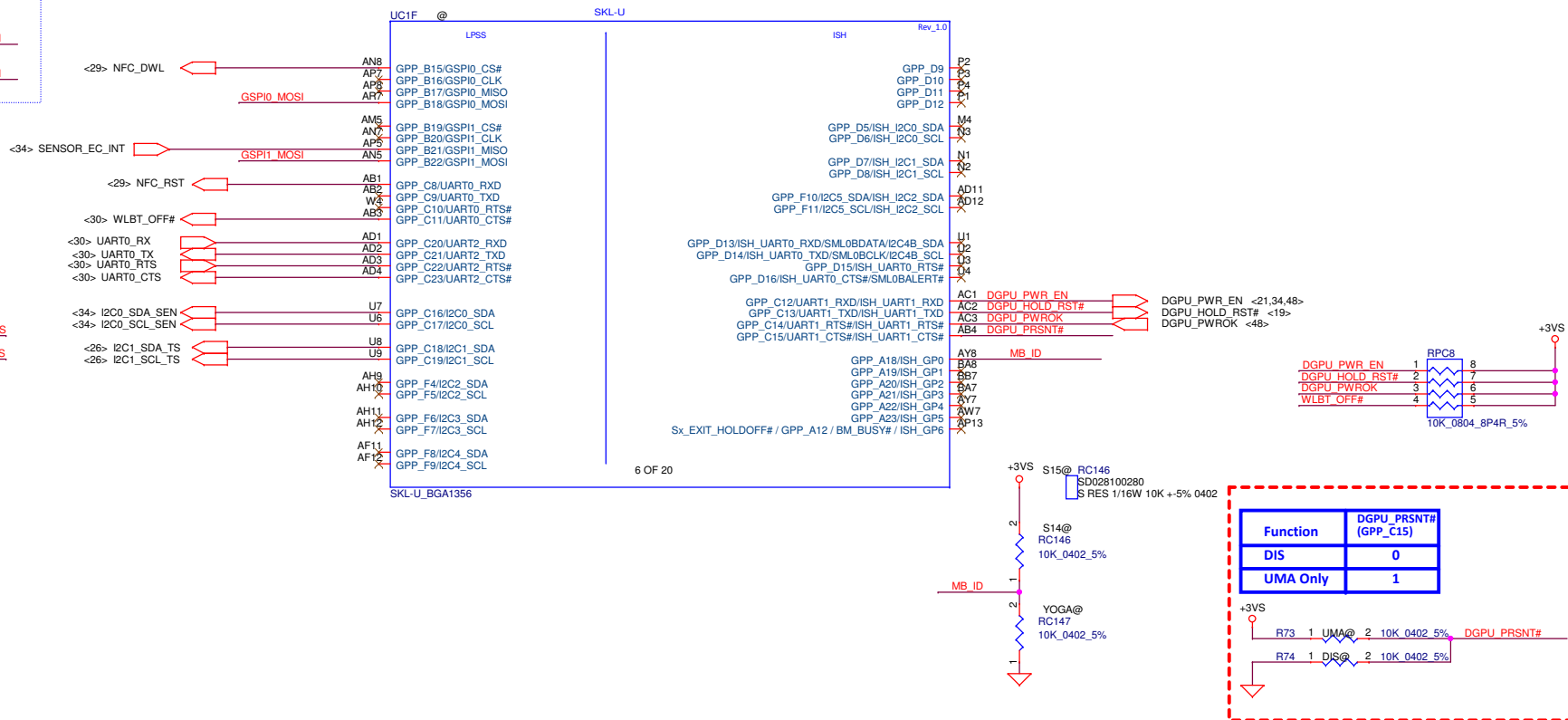
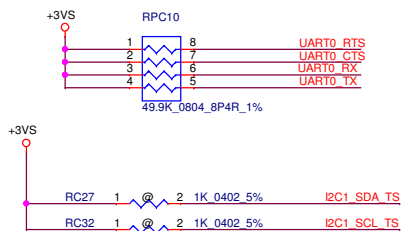
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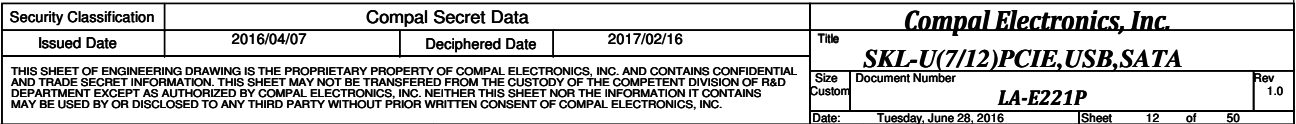


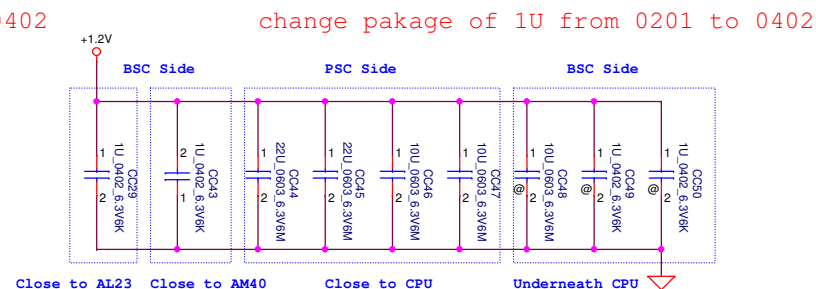
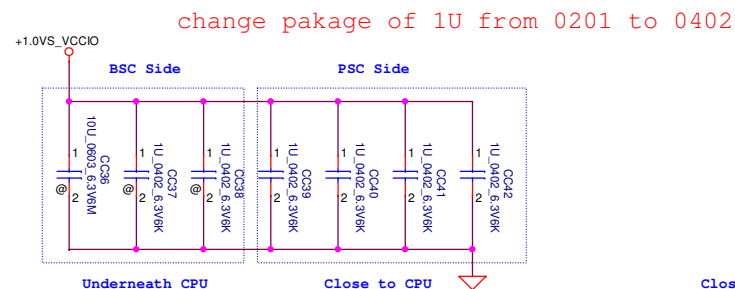
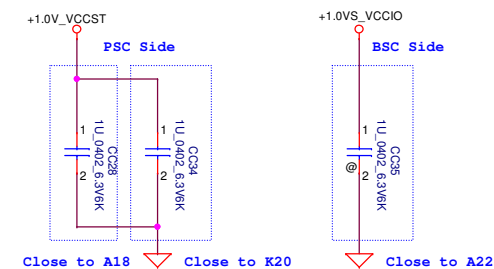
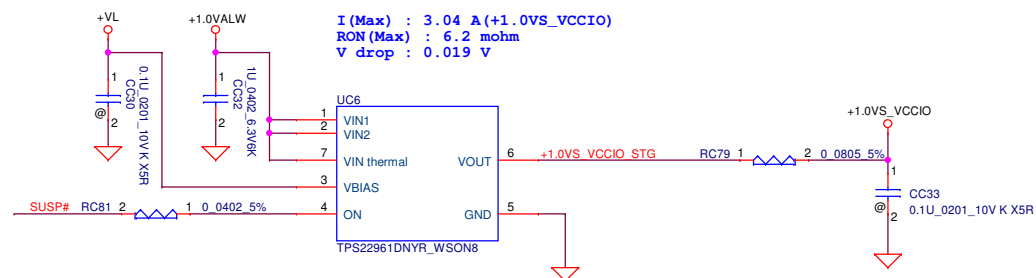
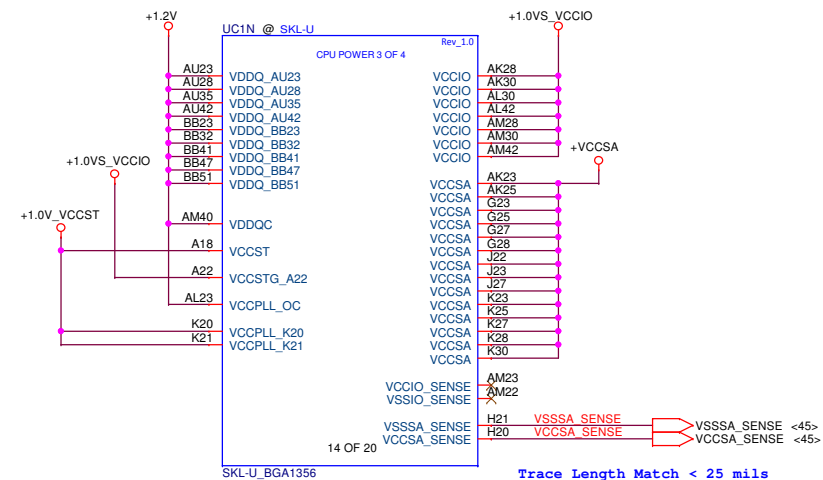
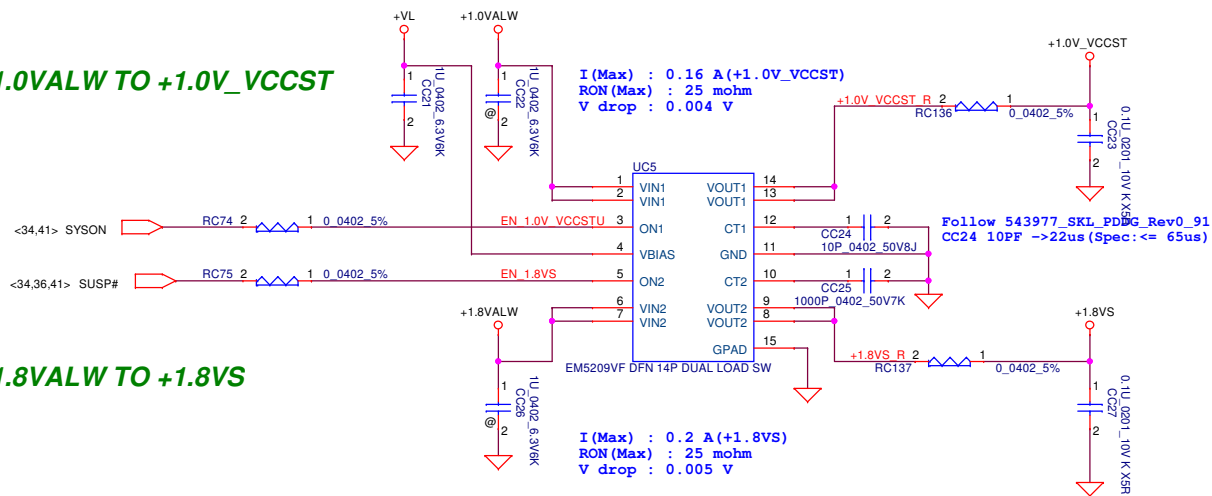
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				SKL-U(S/12)CLK,PM,GPIO	
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1 = LPC Mode

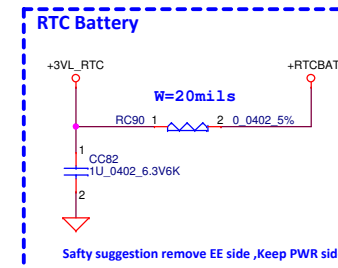
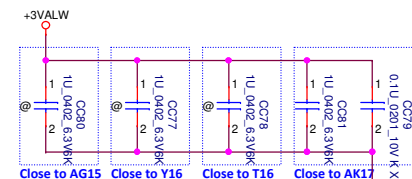
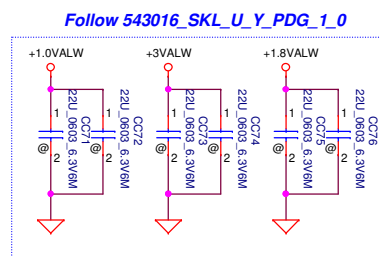
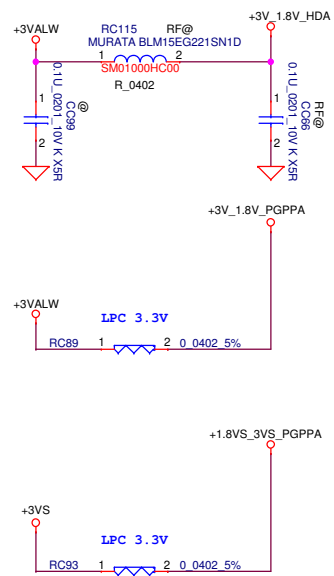


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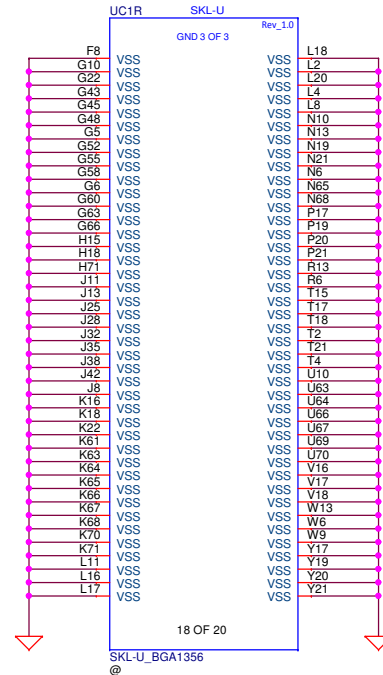
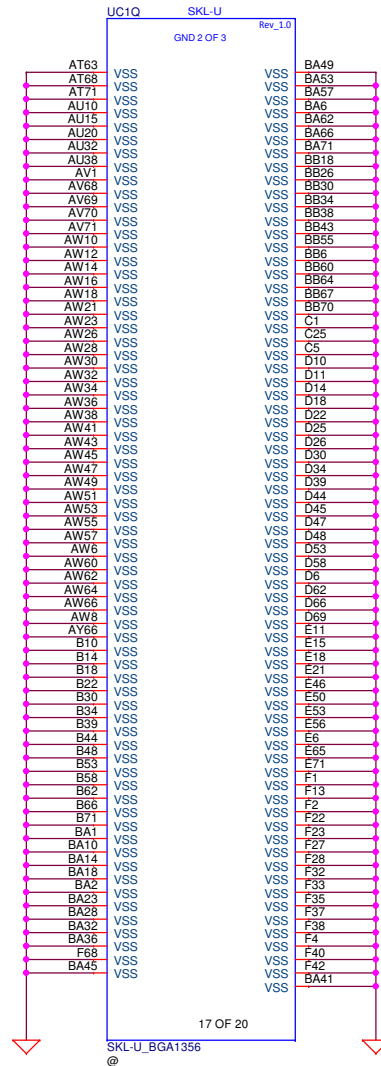
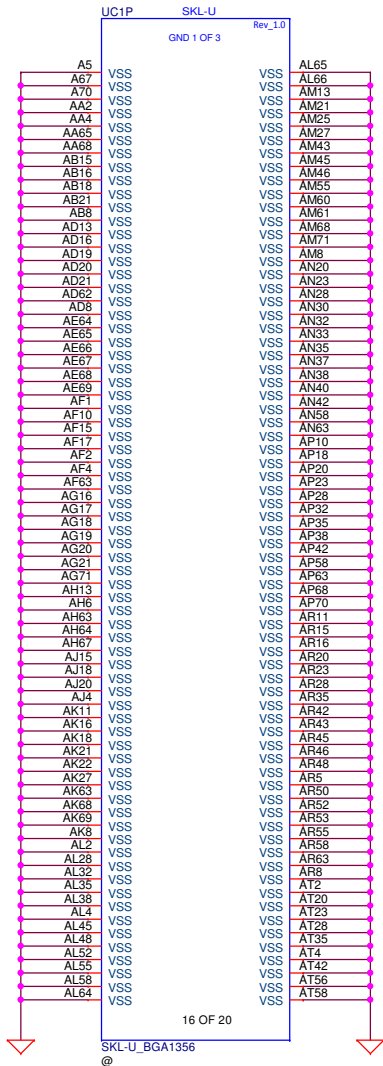




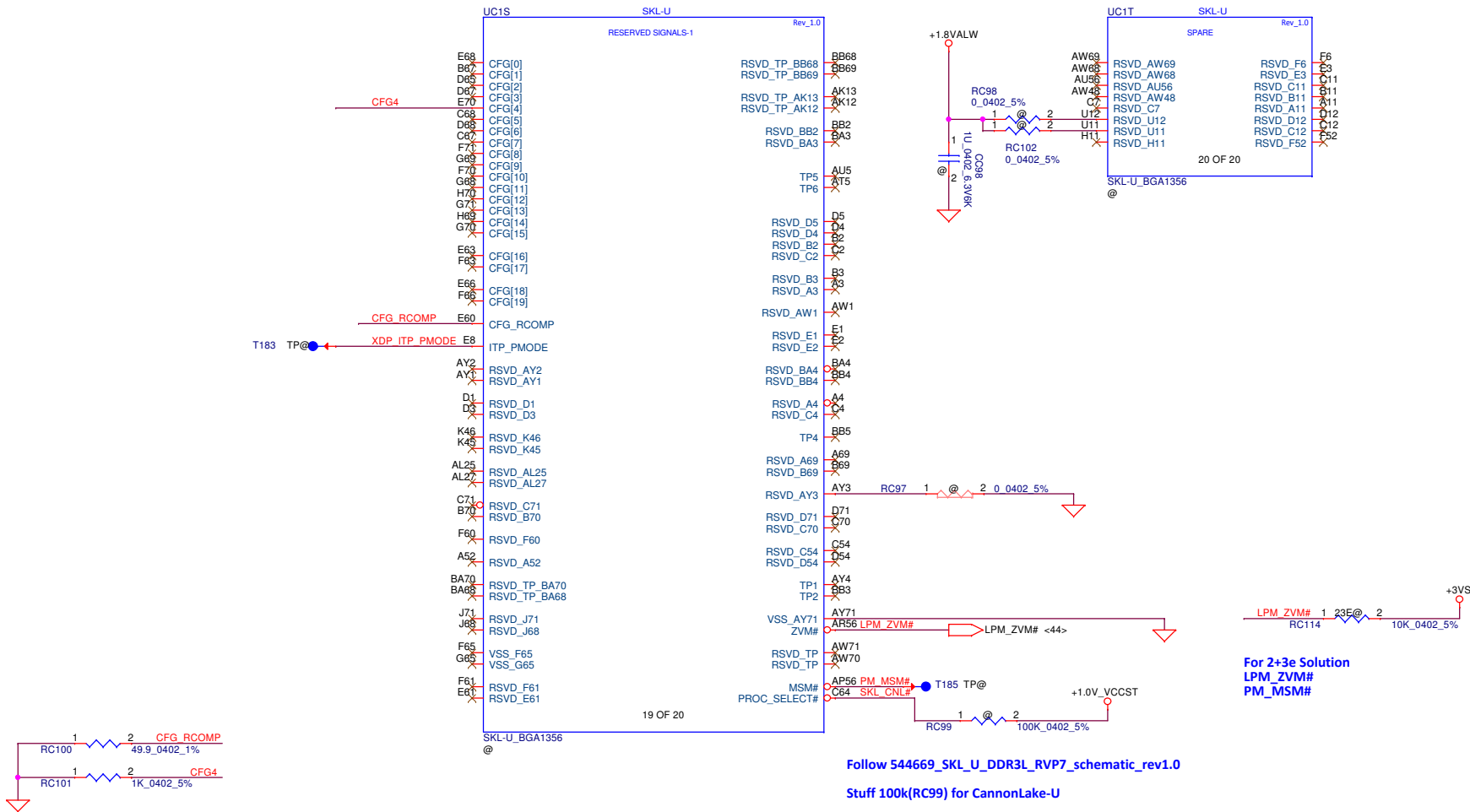
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Display Port Presence Strap

CFG4

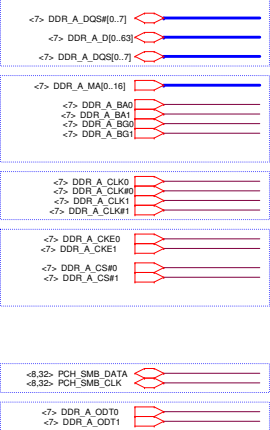
- 1 : Disabled;
No Physical Display Port attached to Embedded Display Port
- 0 : Enabled;
An external Display Port device is connected to the Embedded Display Port

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Interleaved Memory

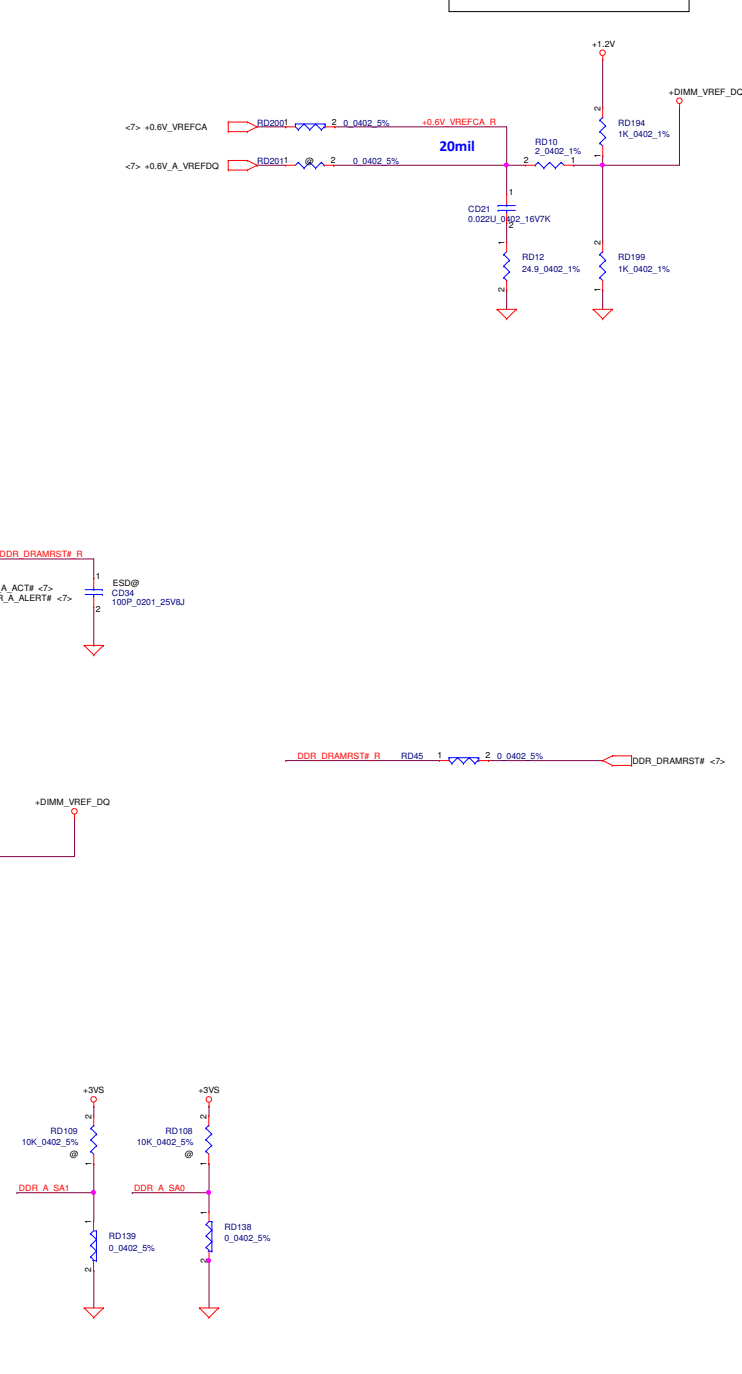
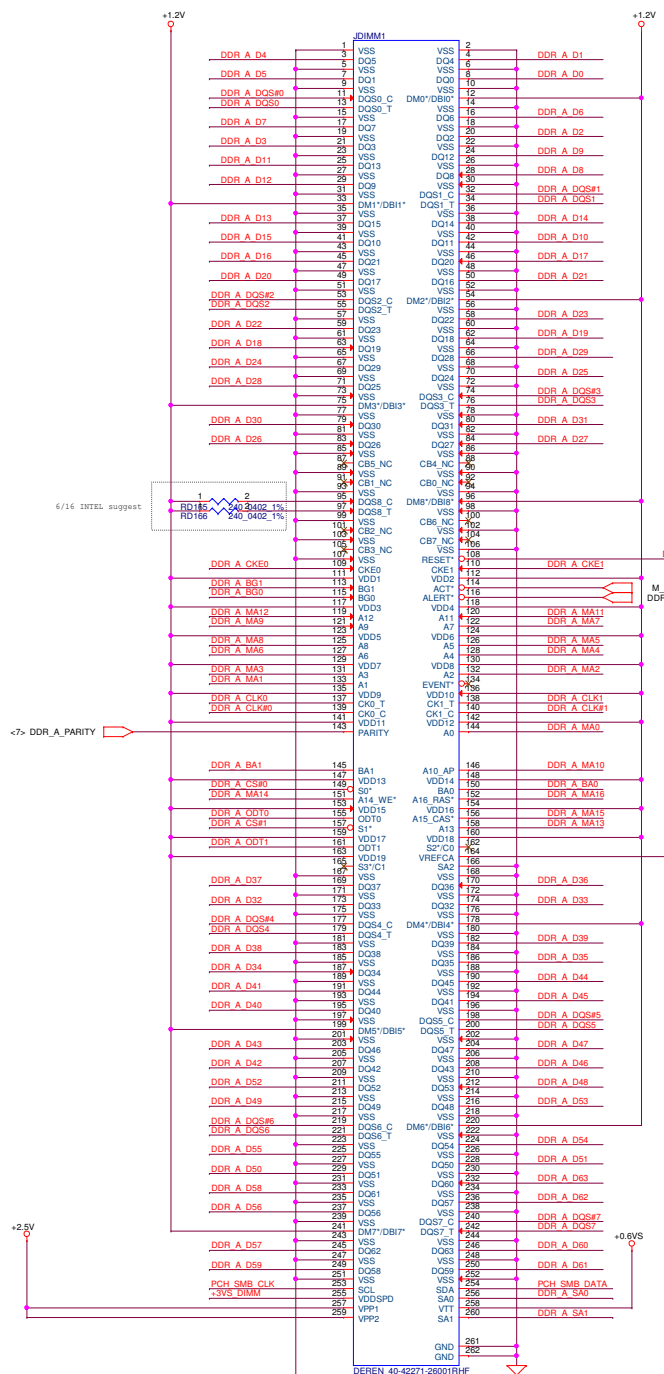
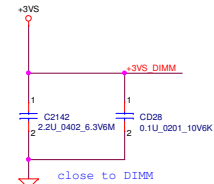
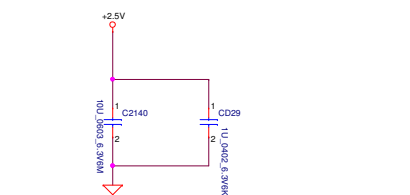
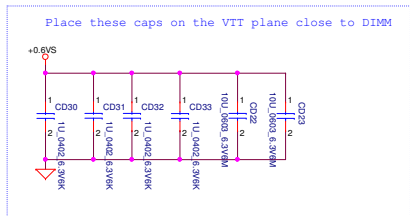
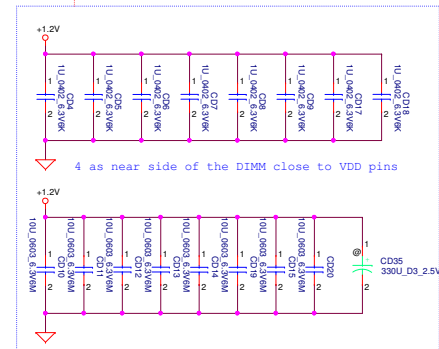
Reverse Type

2-3A to 1 DIMMs/channel

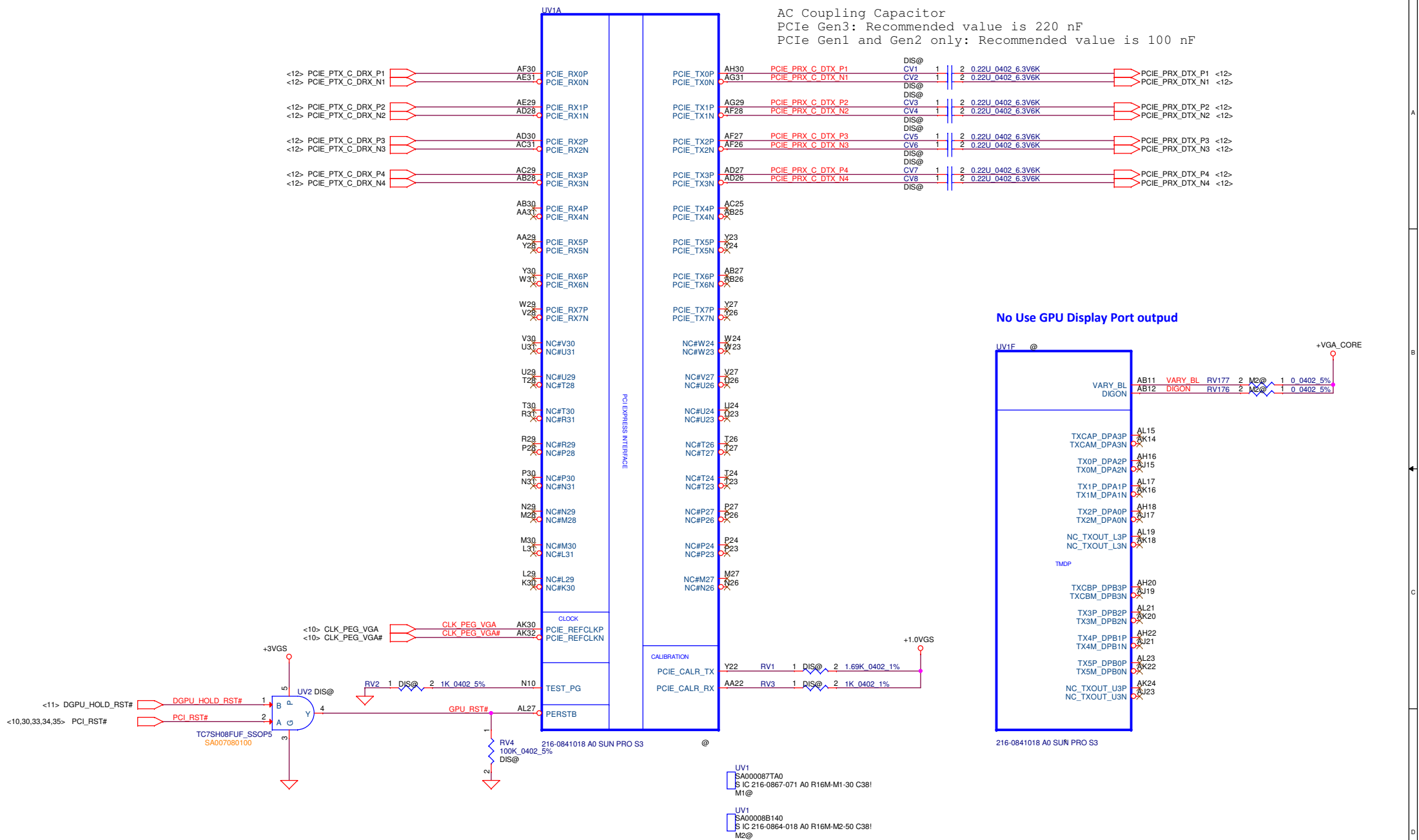


Layout Note:
Place near JDIMM1

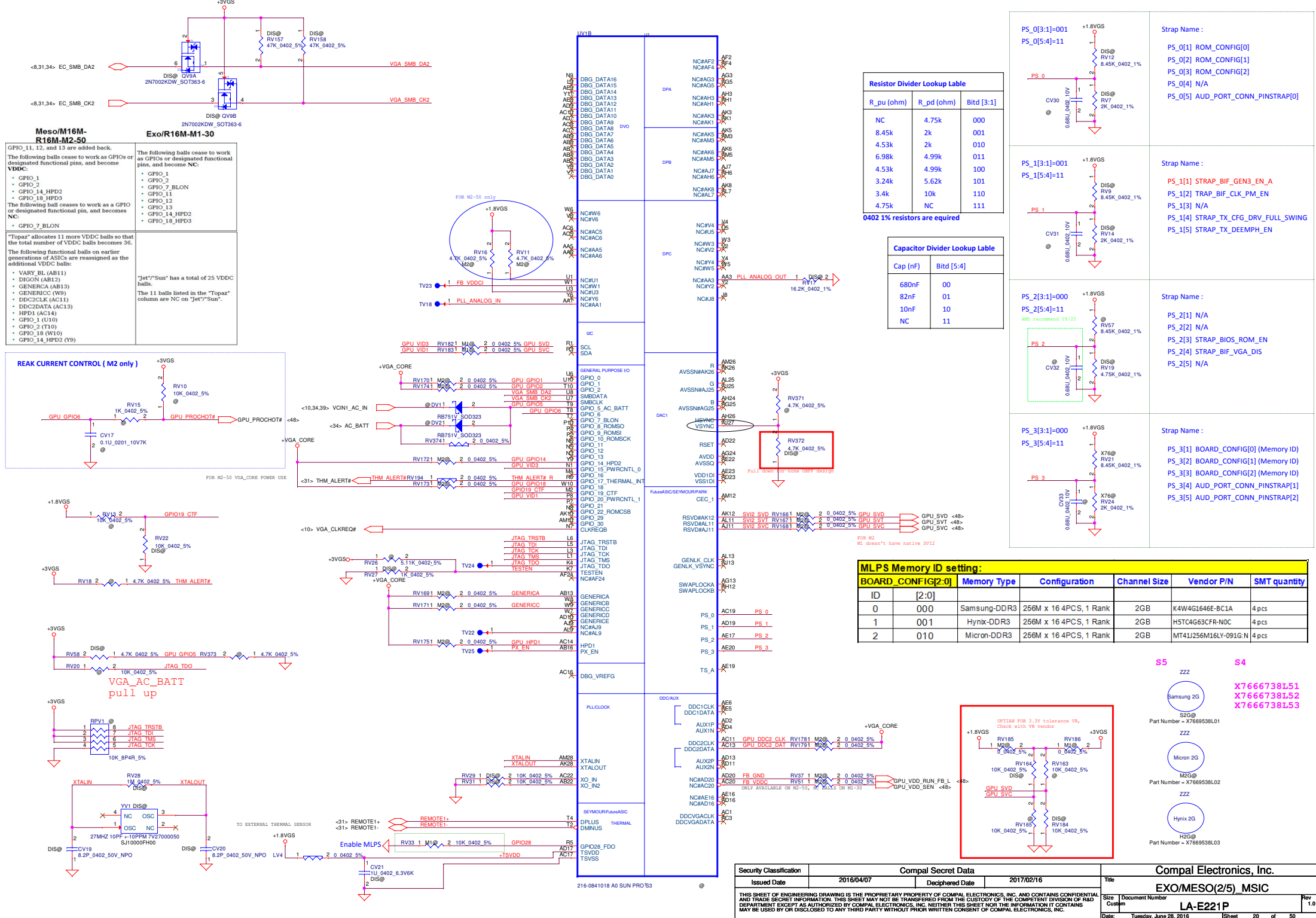
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



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Meso/M16M-R16M-M2-50

The following balls cease to work as GPIOs or designated functional pins, and become VDDC:

- GPIO_1
- GPIO_2
- GPIO_14_HPD2
- GPIO_18_HPD3

The following ball ceases to work as a GPIO or designated functional pin, and becomes NC:

- GPIO_7_BLON

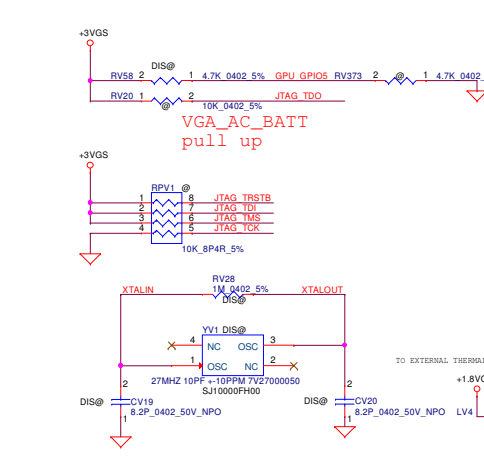
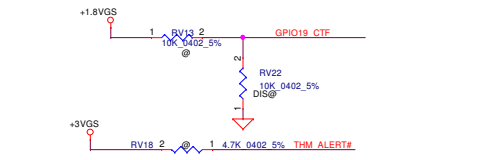
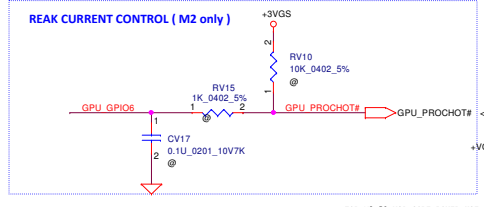
The following balls cease to work as GPIOs or designated functional pins, and become NC:

- GPIO_1
- GPIO_2
- GPIO_7_BLON
- GPIO_11
- GPIO_12
- GPIO_13
- GPIO_14_HPD2
- GPIO_18_HPD3

"Topaz" allocates 11 more VDDC balls so that the total number of VDDC balls becomes 36. The following functional balls on earlier generations of ASICs are reassigned as the additional VDDC balls:

- VARY_BL (AB11)
- DIGON (AB12)
- GENERCA (AB13)
- GENERICC (W9)
- DDC2CLK (AC11)
- DDC2DATA (AC13)
- HPD1 (AC14)
- GPIO_1 (U10)
- GPIO_2 (T10)
- GPIO_18 (W10)
- GPIO_14_HPD2 (Y9)

"Jet"/"Sun" has a total of 25 VDDC balls. The 11 balls listed in the "Topaz" column are NC on "Jet"/"Sun".



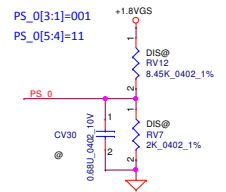
Resistor Divider Lookup Table

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

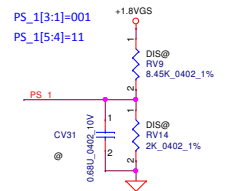
Capacitor Divider Lookup Table

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



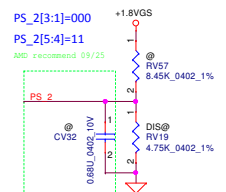
Strap Name :

- PS_0[1] ROM_CONFIG[0]
- PS_0[2] ROM_CONFIG[1]
- PS_0[3] ROM_CONFIG[2]
- PS_0[4] N/A
- PS_0[5] AUD_PORT_CONN_PINSTRAP[0]



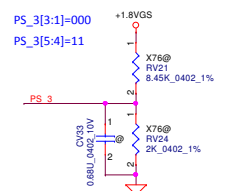
Strap Name :

- PS_1[1] STRAP_BIF_GEN3_EN_A
- PS_1[2] TRAP_BIF_CLK_PM_EN
- PS_1[3] N/A
- PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
- PS_1[5] STRAP_TX_DEEMPH_EN



Strap Name :

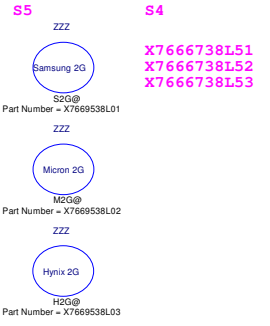
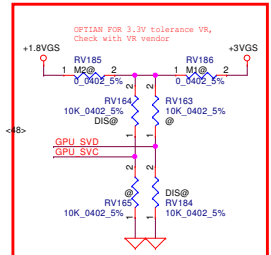
- PS_2[1] N/A
- PS_2[2] N/A
- PS_2[3] STRAP_BIOS_ROM_EN
- PS_2[4] STRAP_BIF_VGA_DIS
- PS_2[5] N/A



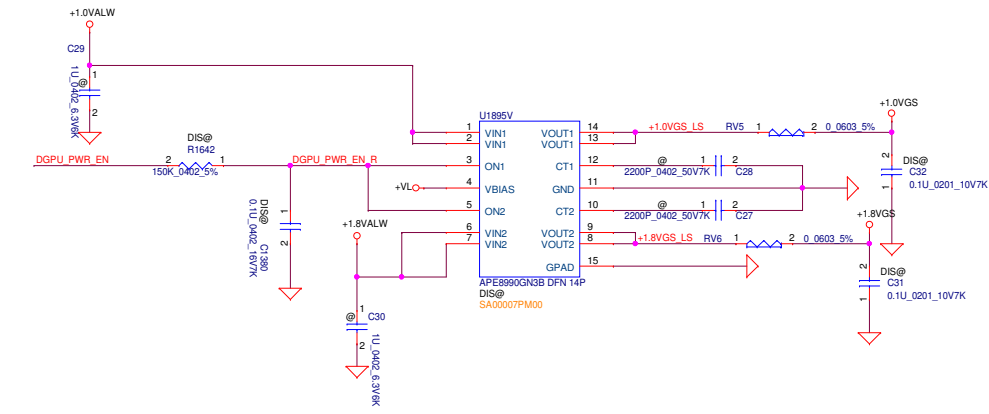
Strap Name :

- PS_3[1] BOARD_CONFIG[0] (Memory ID)
- PS_3[2] BOARD_CONFIG[1] (Memory ID)
- PS_3[3] BOARD_CONFIG[2] (Memory ID)
- PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
- PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

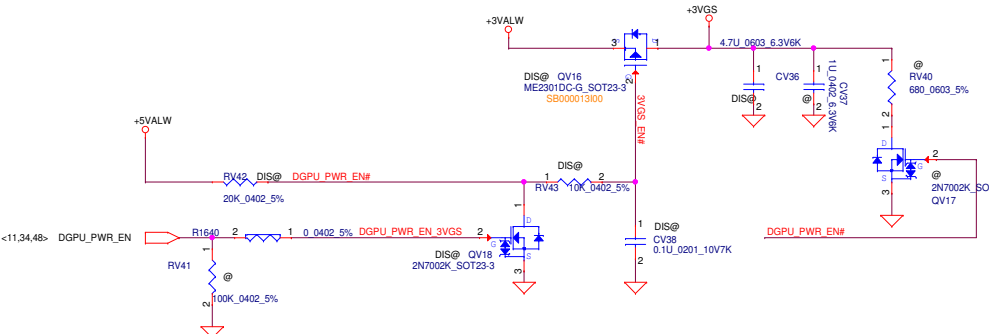
MLPS Memory ID setting:						
BOARD_CONFIG[2:0]		Memory Type	Configuration	Channel Size	Vendor P/N	SMT quantity
ID	[2:0]					
0	000	Samsung-DDR3	256M x 16 4PCS, 1 Rank	2GB	K4W4G1646E-BC1A	4 pcs
1	001	Hynix-DDR3	256M x 16 4PCS, 1 Rank	2GB	H5TC4G63CFR-NOC	4 pcs
2	010	Micron-DDR3	256M x 16 4PCS, 1 Rank	2GB	MT41J256M16LY-091G:N	4 pcs



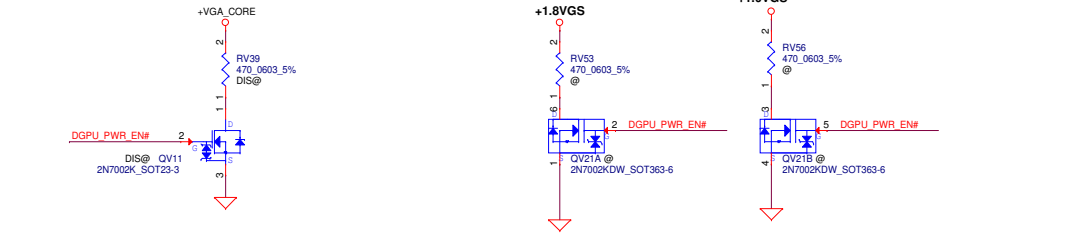
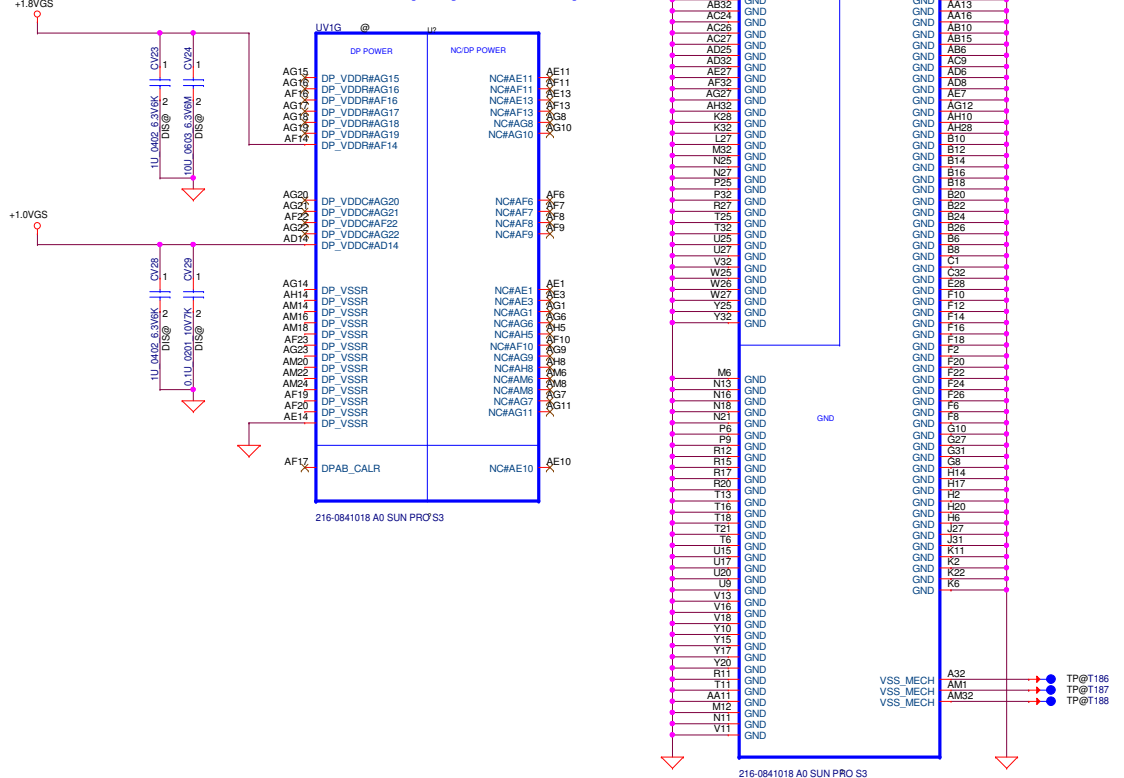
+1.8VALW TO +1.8VGS
+1.0VALW TO +1.0VGS
Load switch



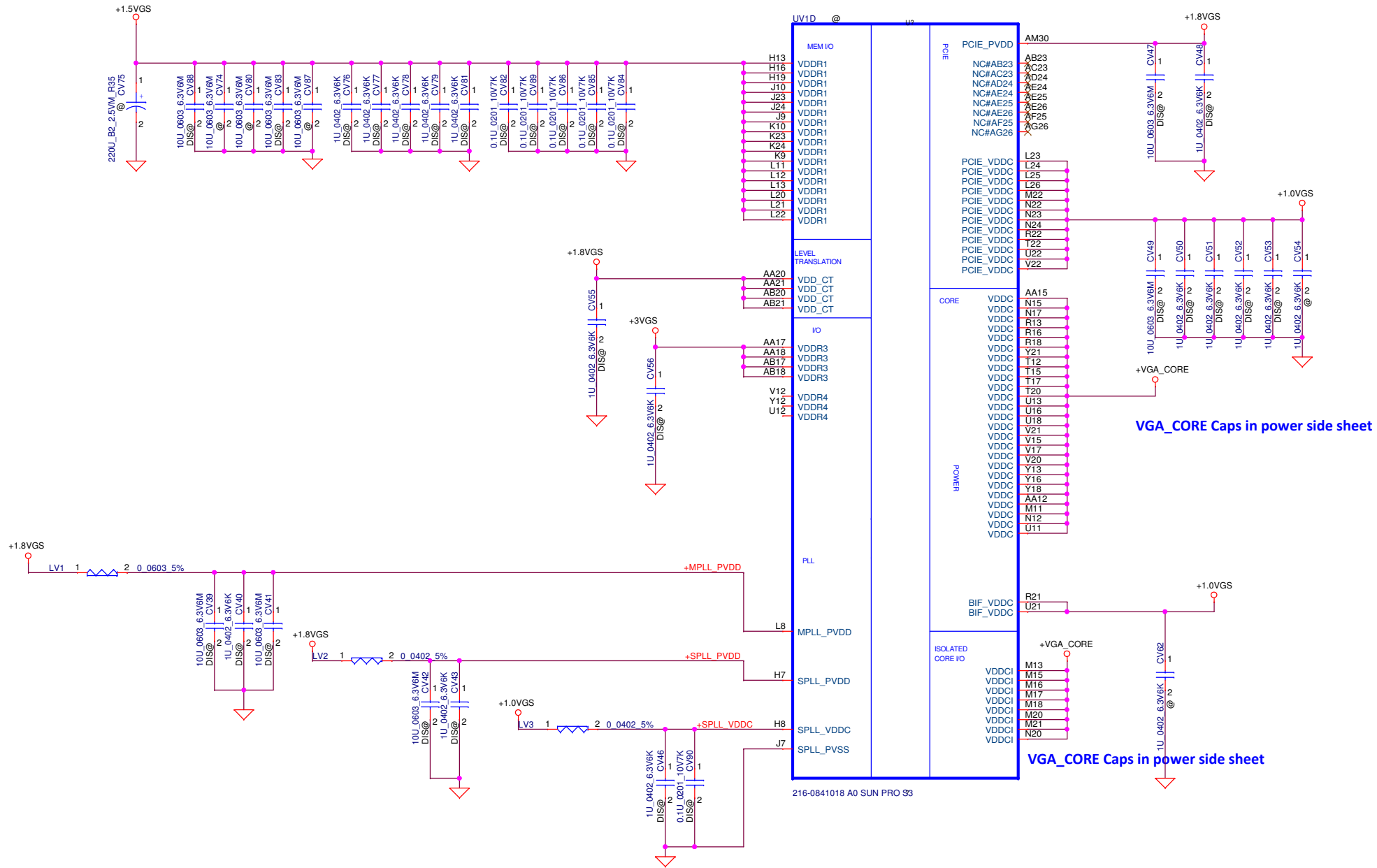
+3VS to +3VGS



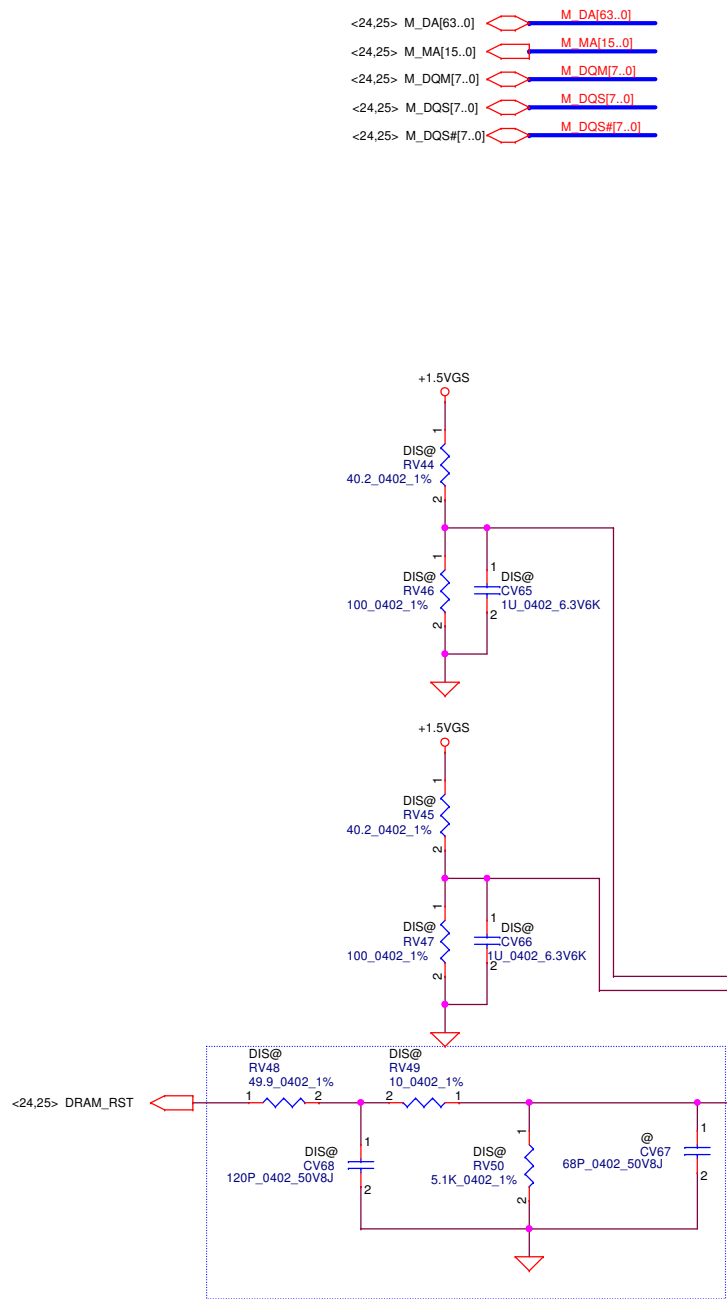
No Use GPU Display Port output



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Size		Document Number		Rev	
Custom		LA-E221P		1.0	
Date:		Tuesday, June 28, 2016		Sheet 21 of 50	



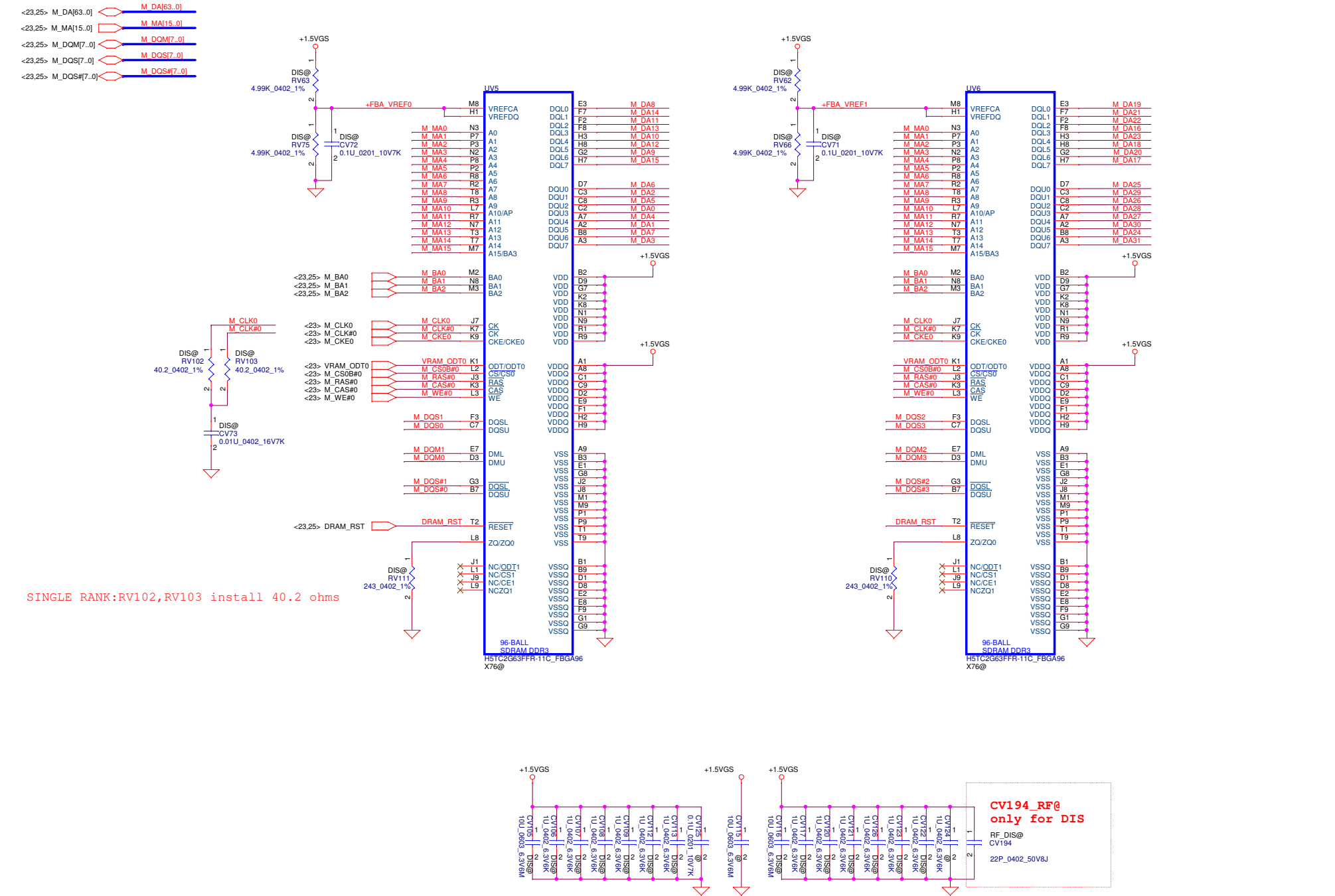
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Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI.

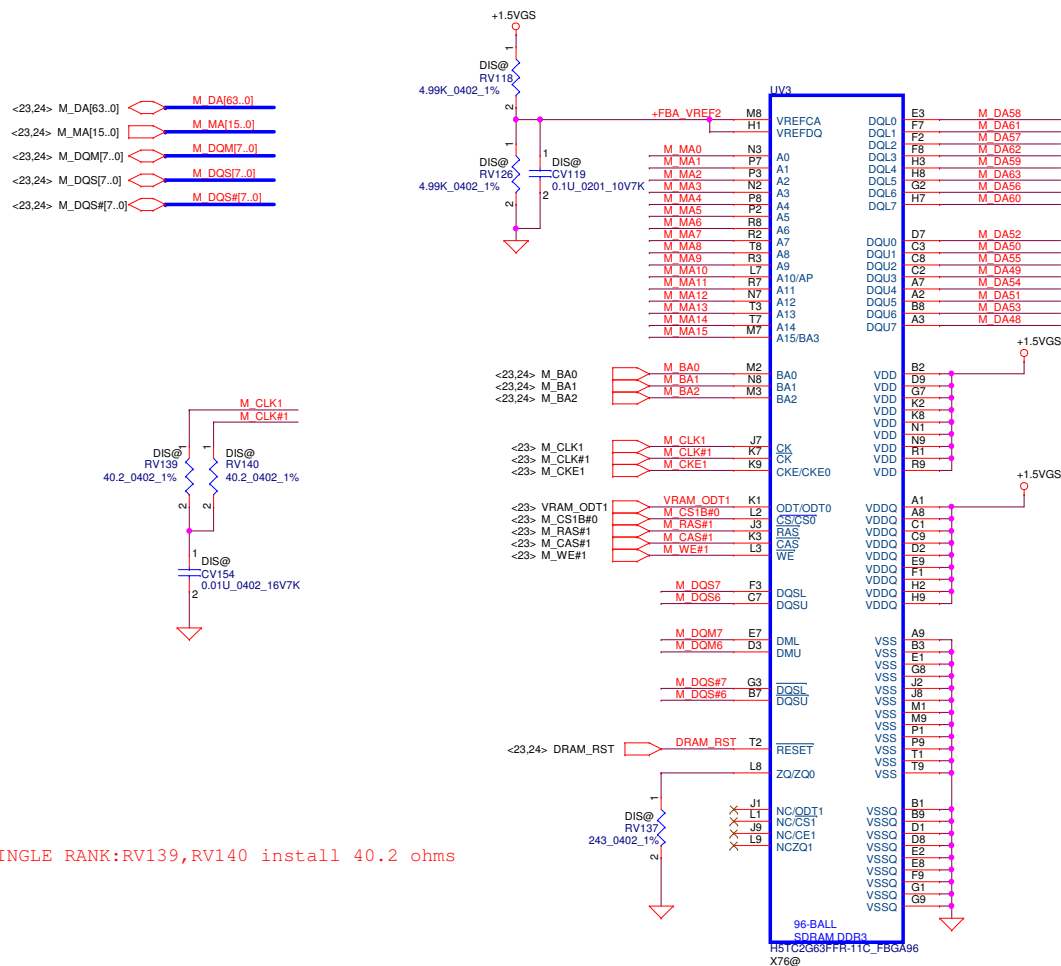
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DDR3 Memory Channel Rank 0:A0

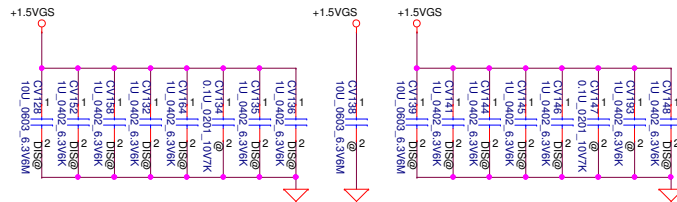
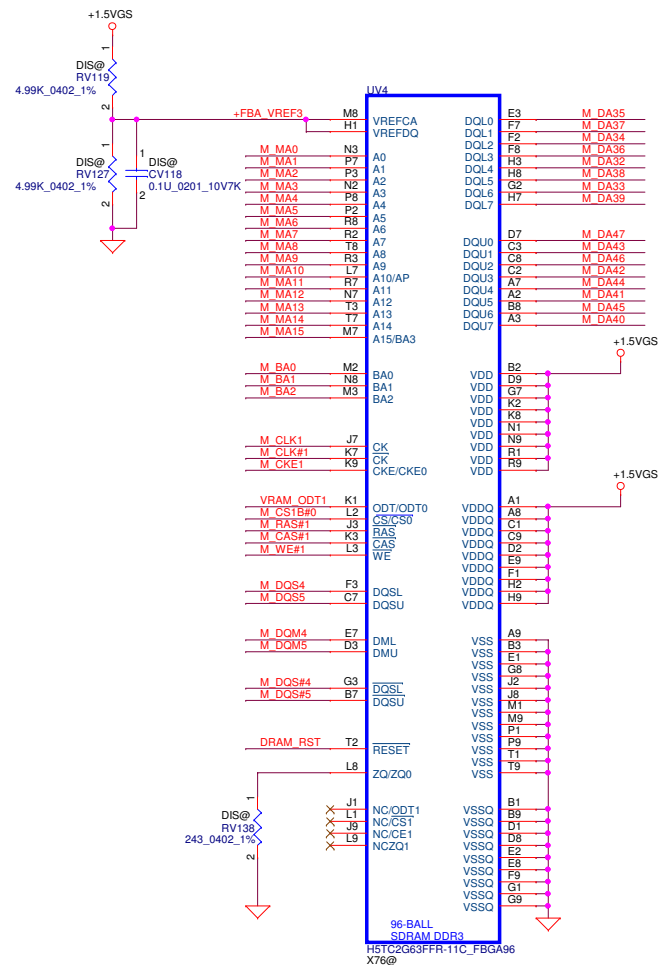


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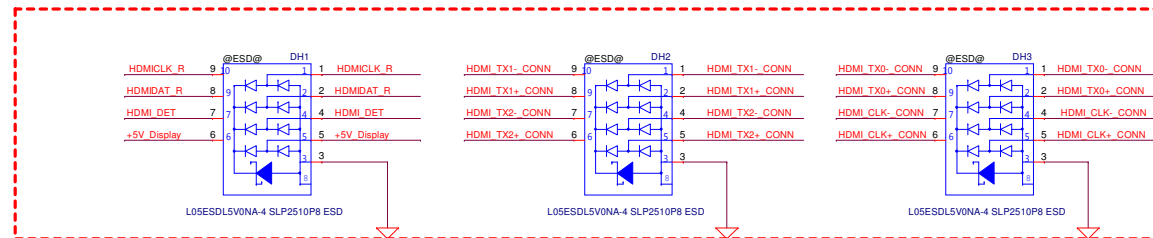
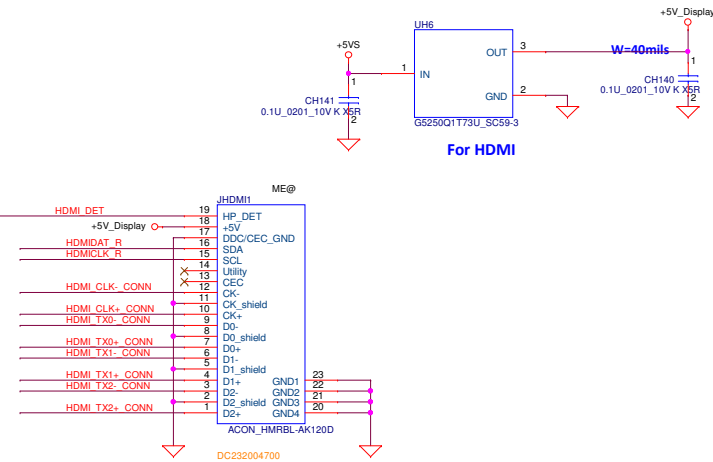
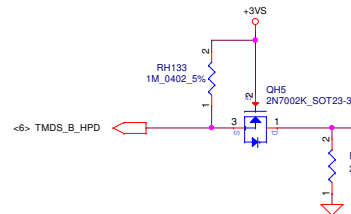
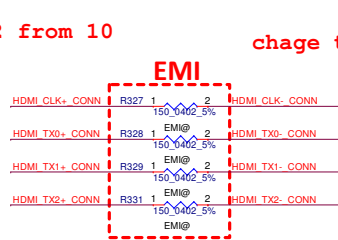
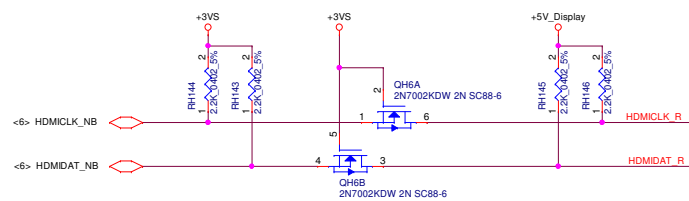
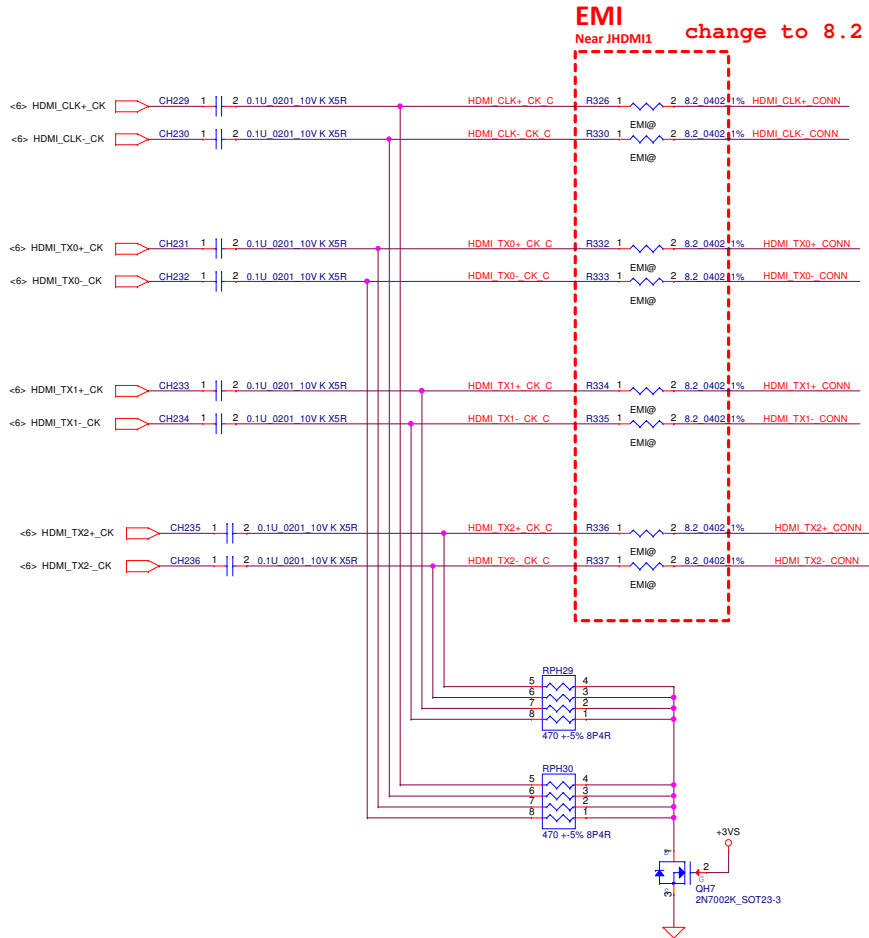
DDR3 Memory Channel Rank 0:A1



SINGLE RANK:RV139,RV140 install 40.2 ohms

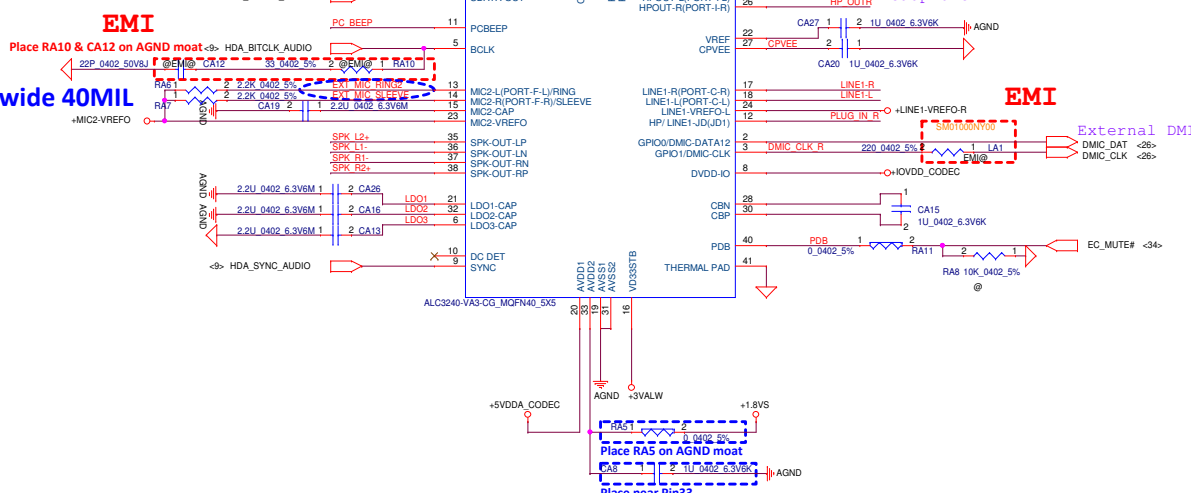


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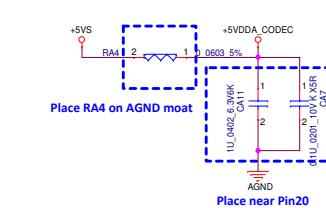


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ALC3240



+5VS → +5VDDA_CODEC



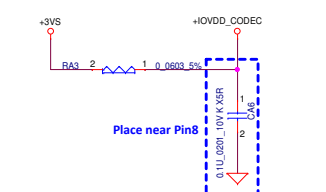
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	
Intel Skylake	X	V	V	V	V

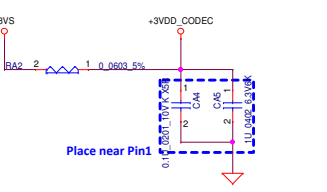
Each Platform HDA Link Voltage Support (Pin 8) :

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

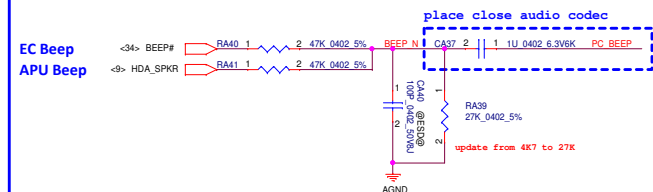
+3VS → +IOVDD_CODEC



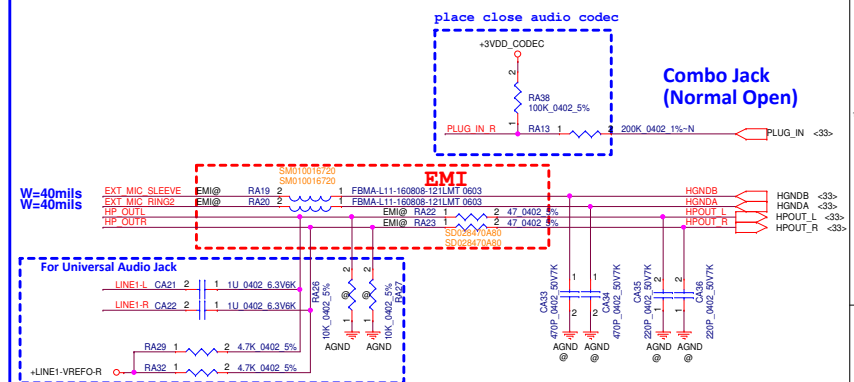
+3VS → +3VDD_CODEC



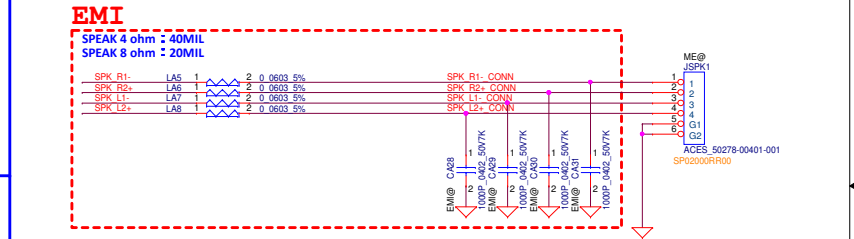
PC BEEP



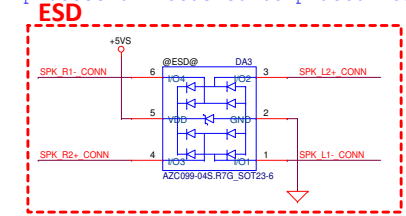
Input



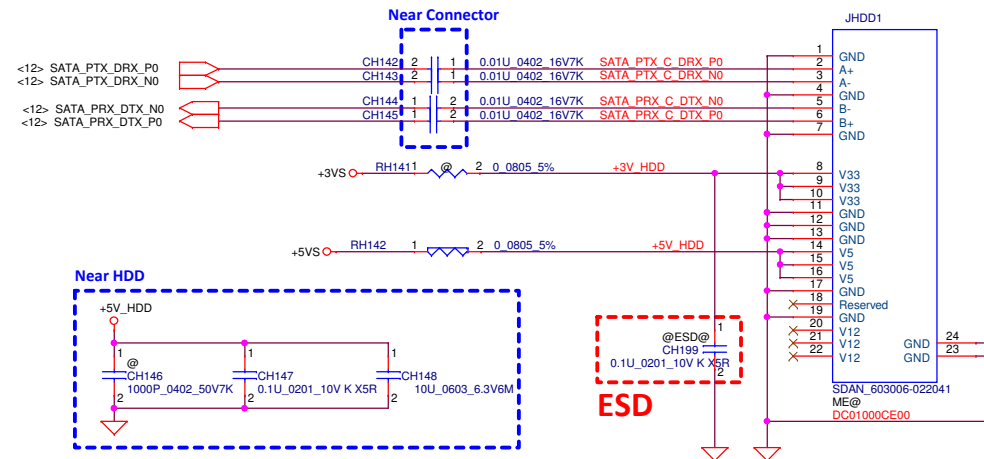
Output



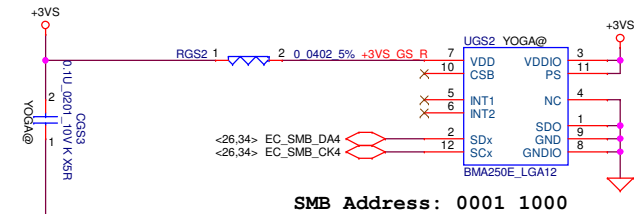
ESD protection needs to be placed near connector side



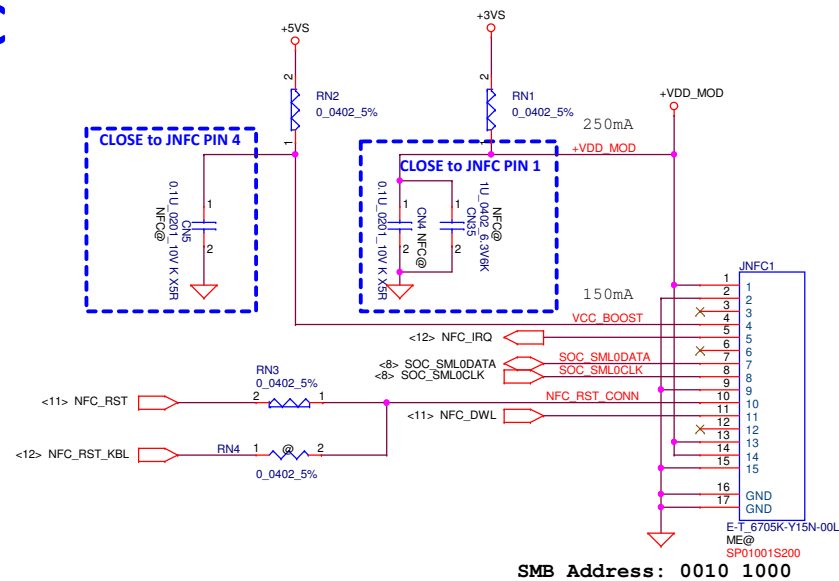
HDD



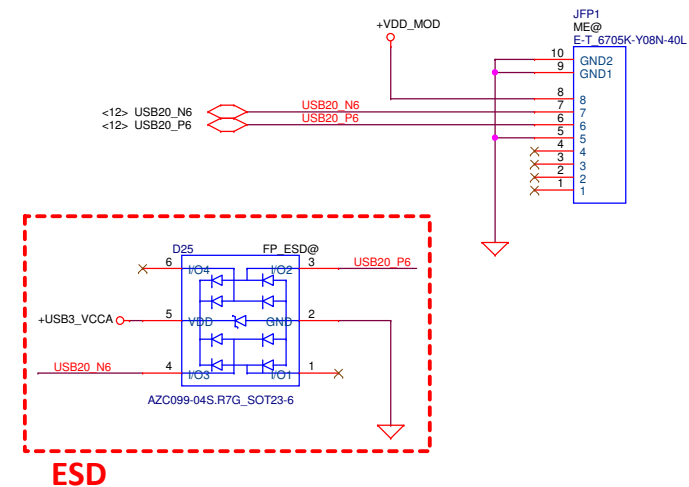
(G-Sensor for 360-degree reverse)



NFC

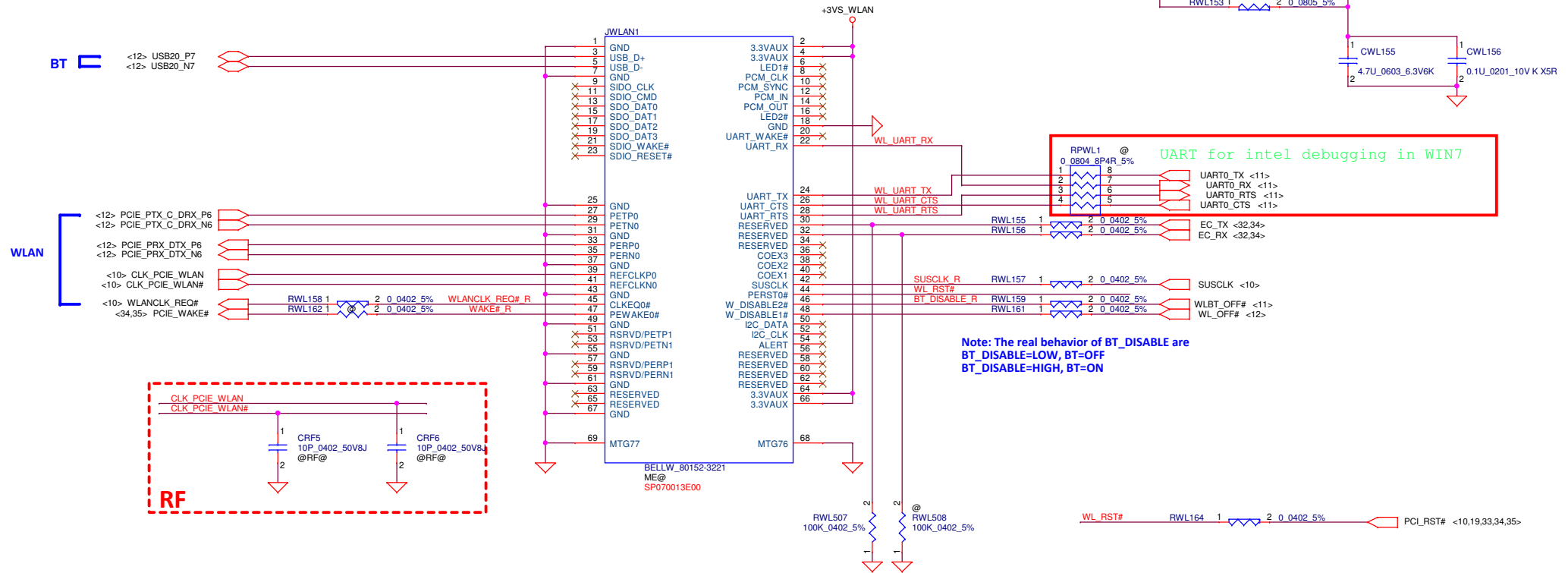


Finger Printer



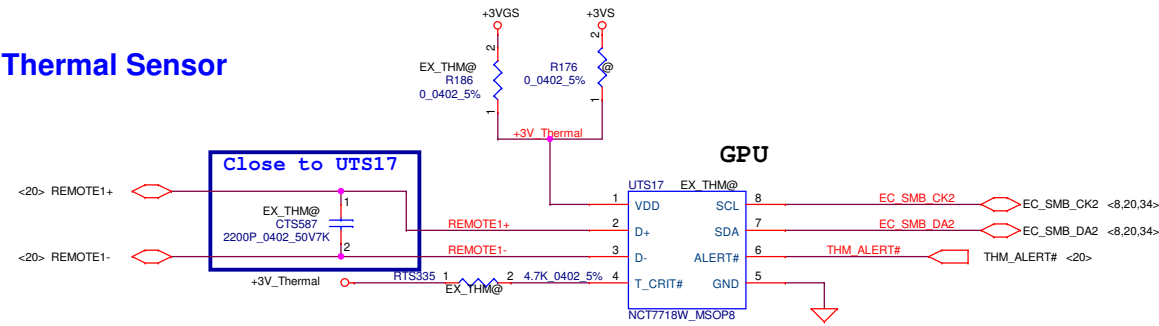
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NGFF for WLAN / BT(Key E)

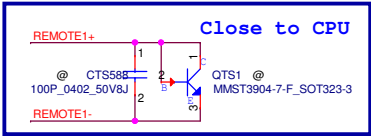


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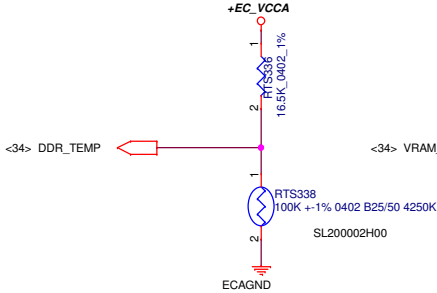
Thermal Sensor



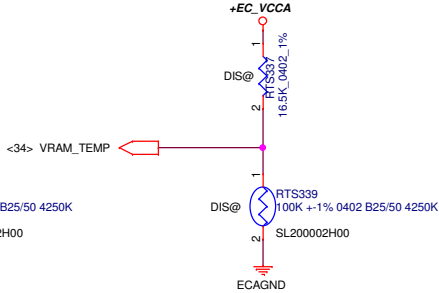
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"



DDR



VRAM



CPU

VGA

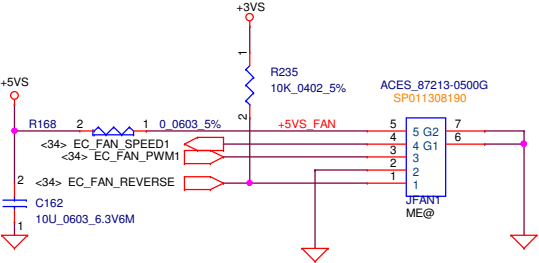
LAN

NGFF

Shielding Clip

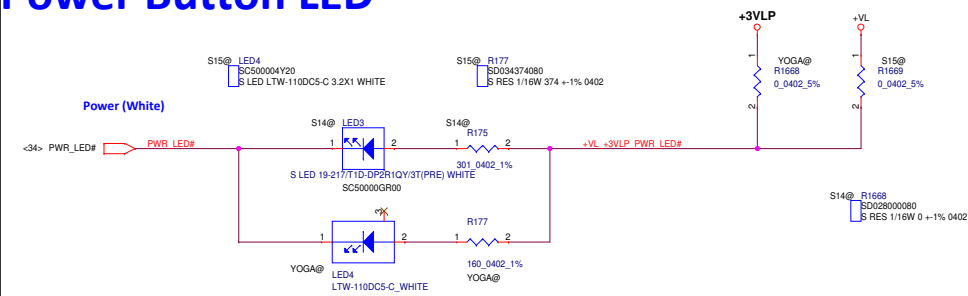
Larger

Smaller

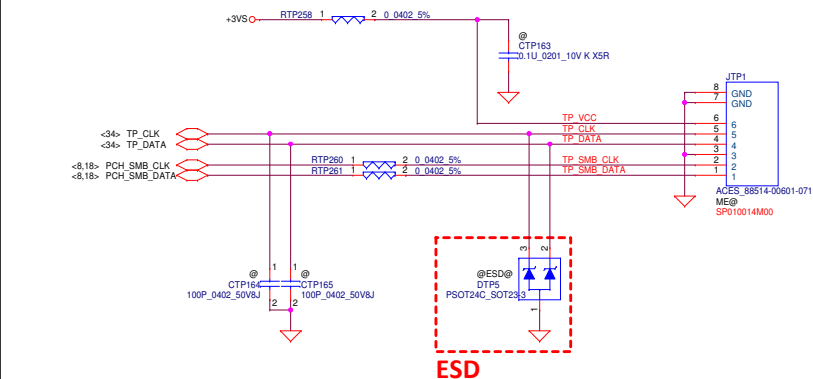


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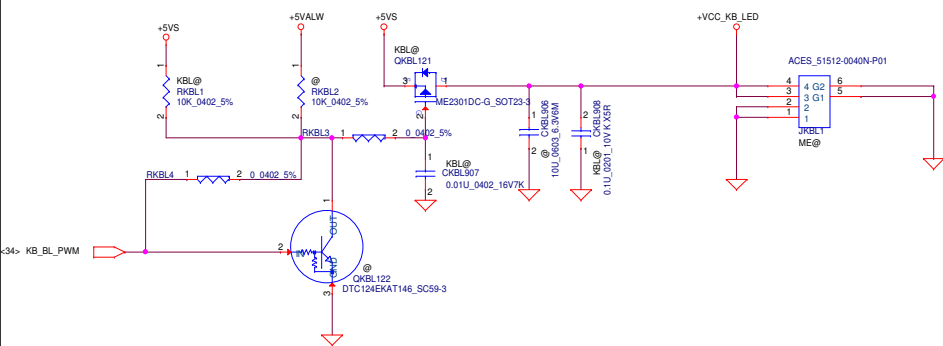
Power Button LED



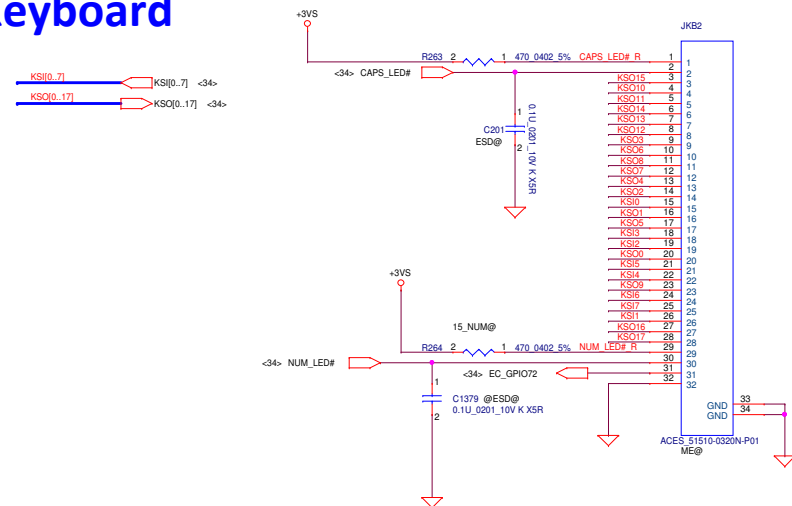
Touch Pad



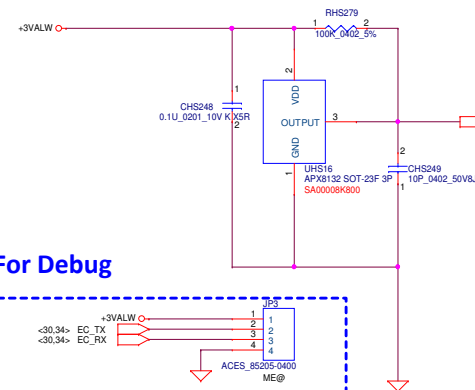
Keyboard Backlight



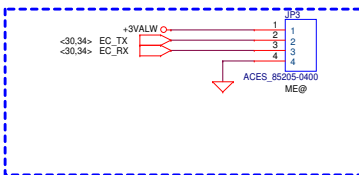
Keyboard



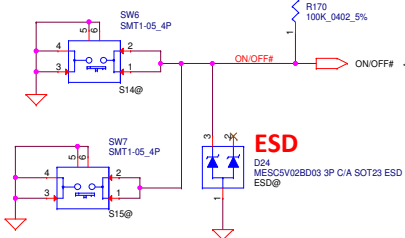
Hall Sensor & Button



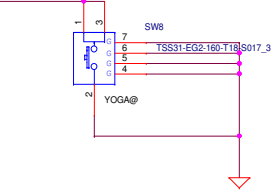
For Debug



Power Button For S Series

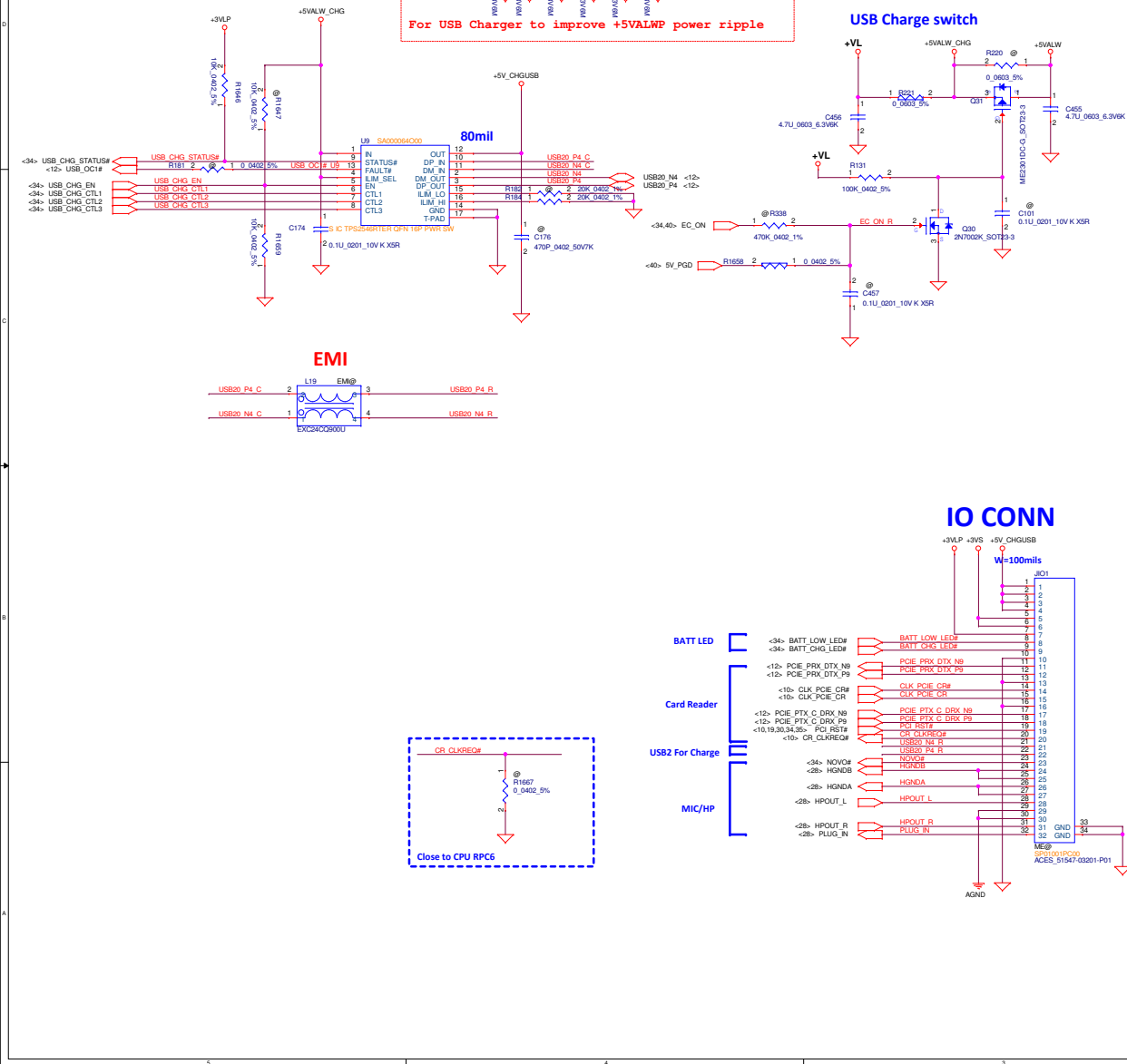


Power Button For YOGA

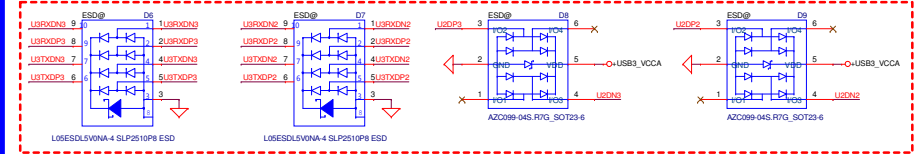


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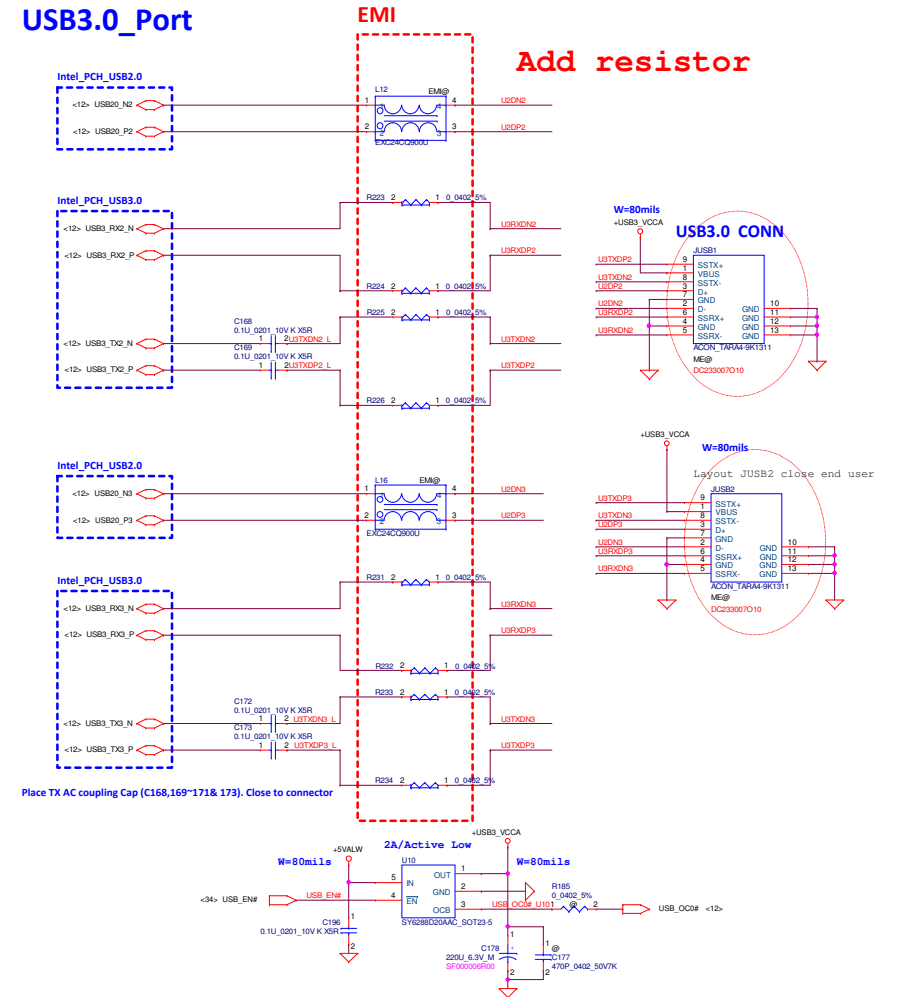
USB Charge



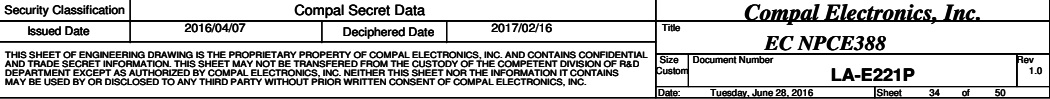
ESD

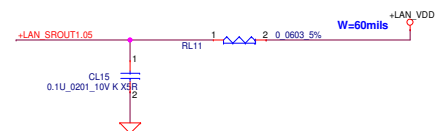


USB3.0_Port



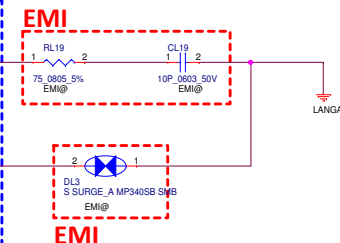
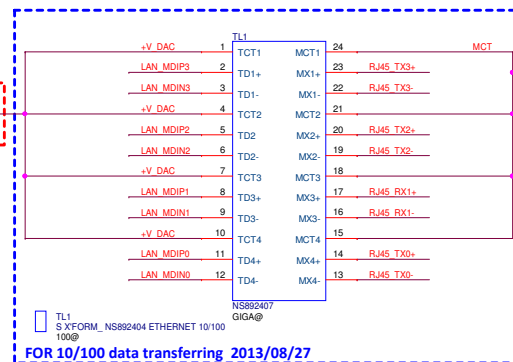
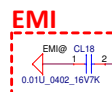
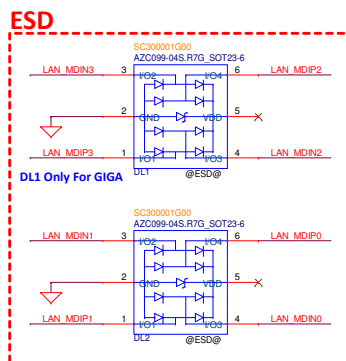
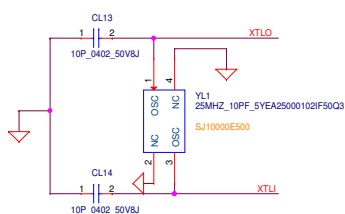
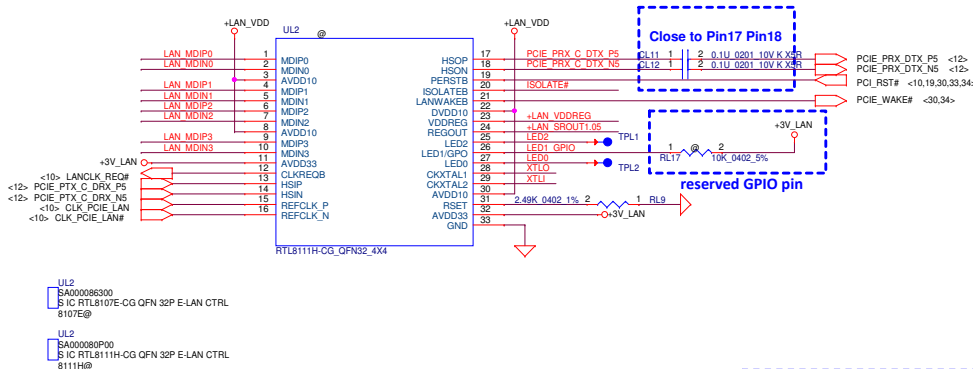
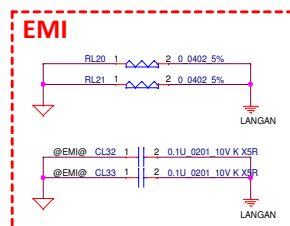
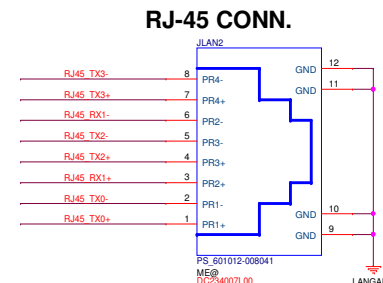
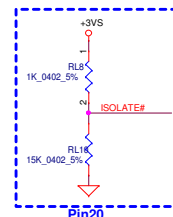
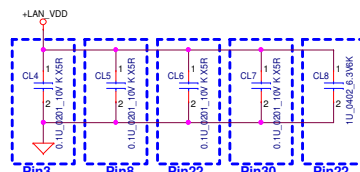
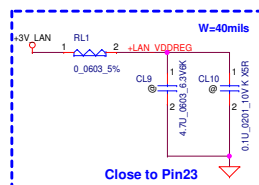
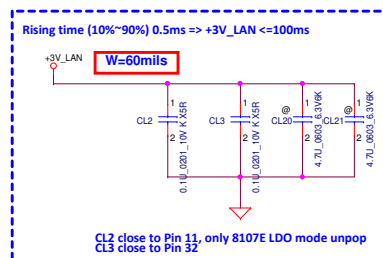
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2016/04/07	Deciphered Date	2017/02/16	USB2/USB3 /FP /IO Board LA-E221P	
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			Sheet	33 of 50	

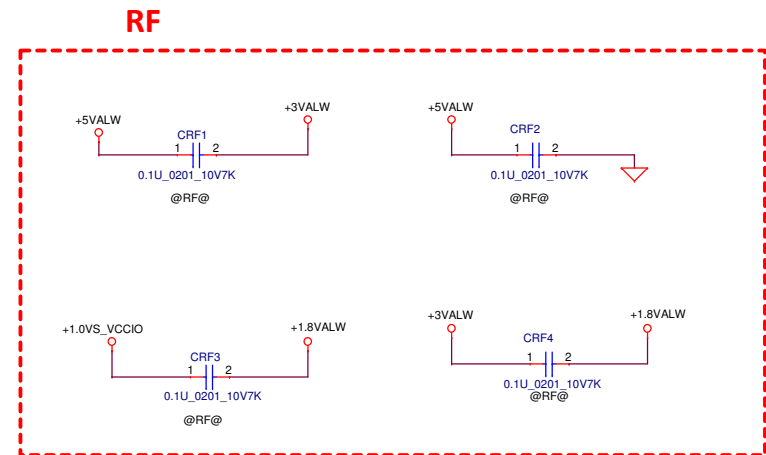
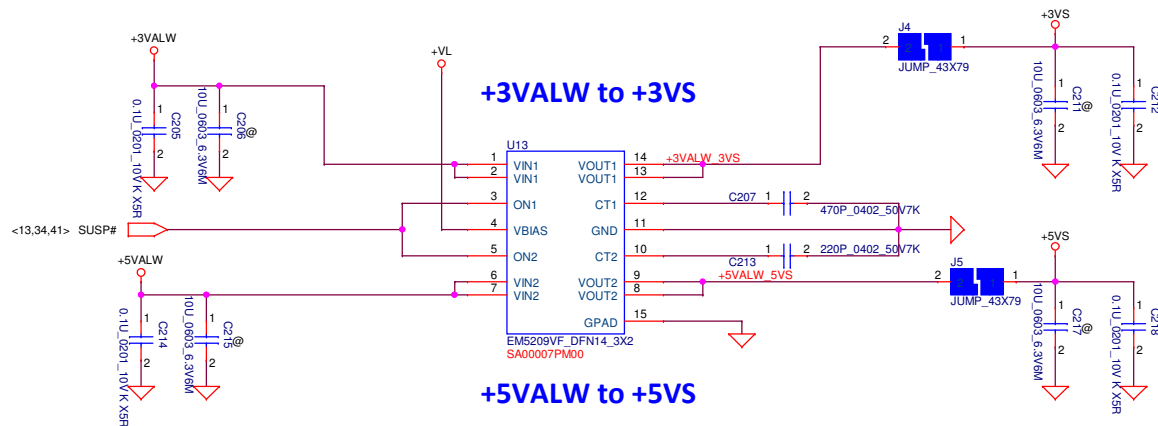




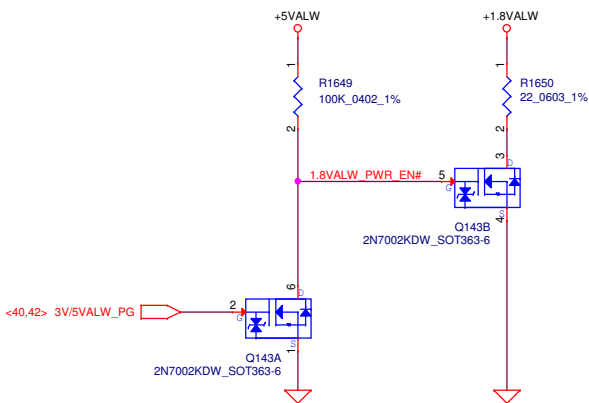
	1.0V Source	RL11	CL15
RTL8111H	LDO	O	O
RTL8107E	LDO	O	O

**LL1, CL16, and CL17 close to Pin24
(Should be place within 200 mils)**

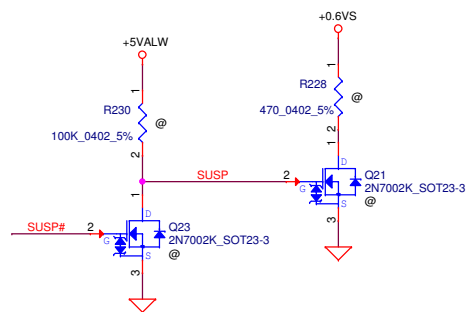




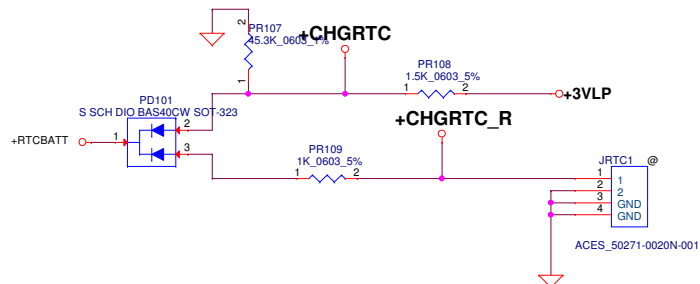
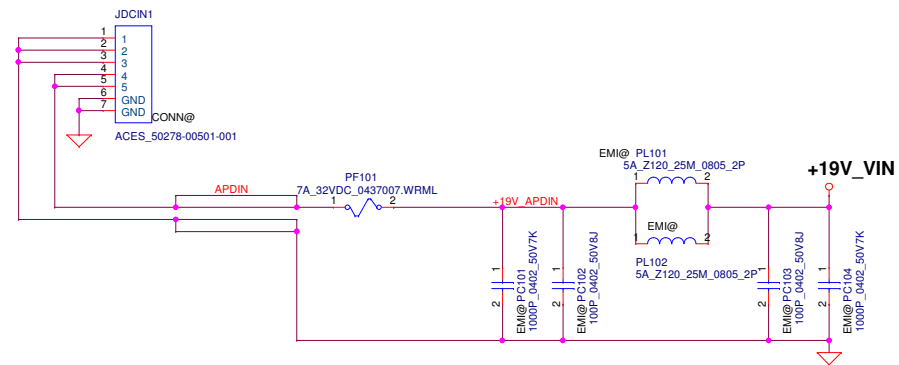
For +1.8VALW Discharge



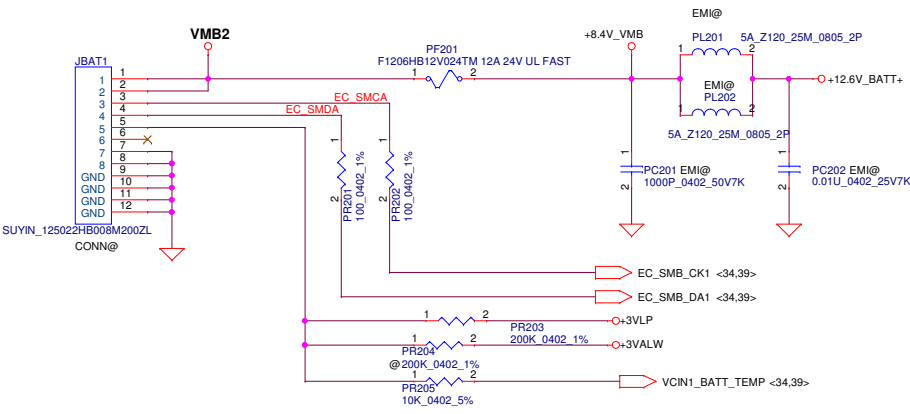
For +0.6VS Discharge



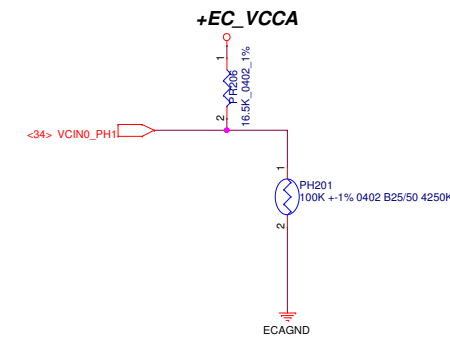
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								DC to DC	
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						Custom	LA-E221P	1.0	
						Date:	Tuesday, June 28, 2016	Sheet	36 of 50



Security Classification	Compal Secret Data			Title	
Issued Date	2015/07/27	Deciphered Date	2016/07/27	PWR- DCIN / Vin Detector	
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				1.0	1.0
				Date: Tuesday, June 28, 2016	Sheet 37 of 50



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

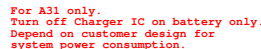


```

Ipsys = KPSYS x ( VADP x IADP + VBAT x IBAT )
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.
-----
adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

```

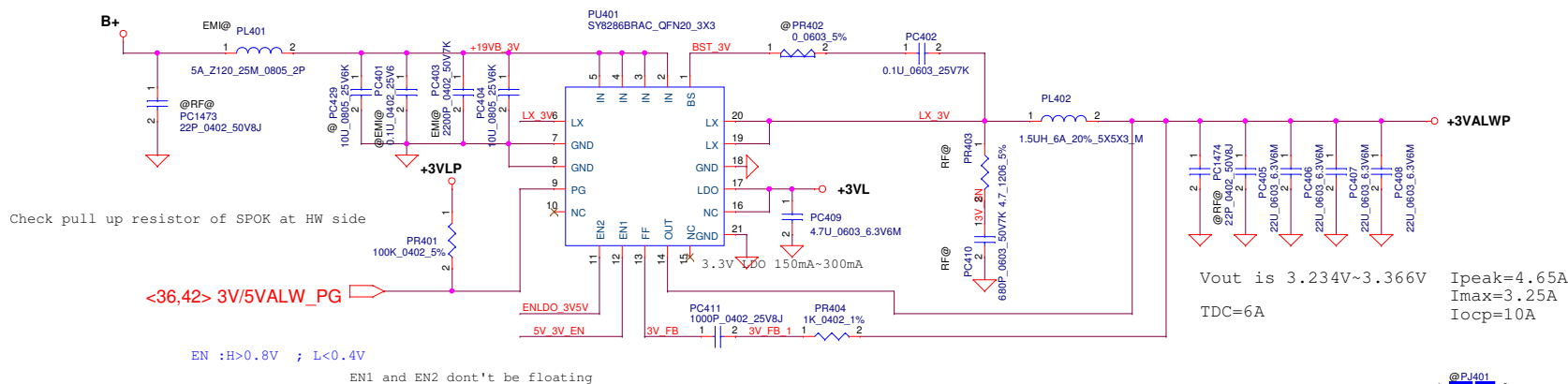
Module model information
ISL95520 Hybrid Boost V2.mdd



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Issued Date	2015/07/27	Deciphered Date	2016/07/27	
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Author	Inspector	Issue No	98	Rev 1.0
			98	1.0

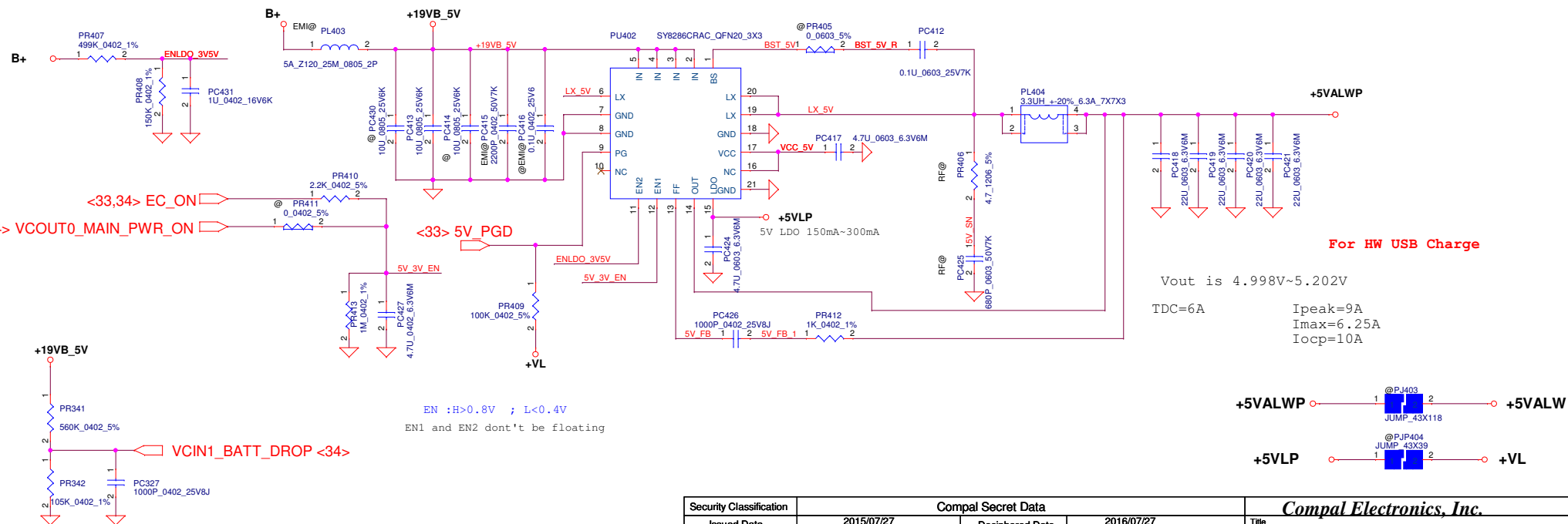
Module model information

SY8286B_V1.mdd

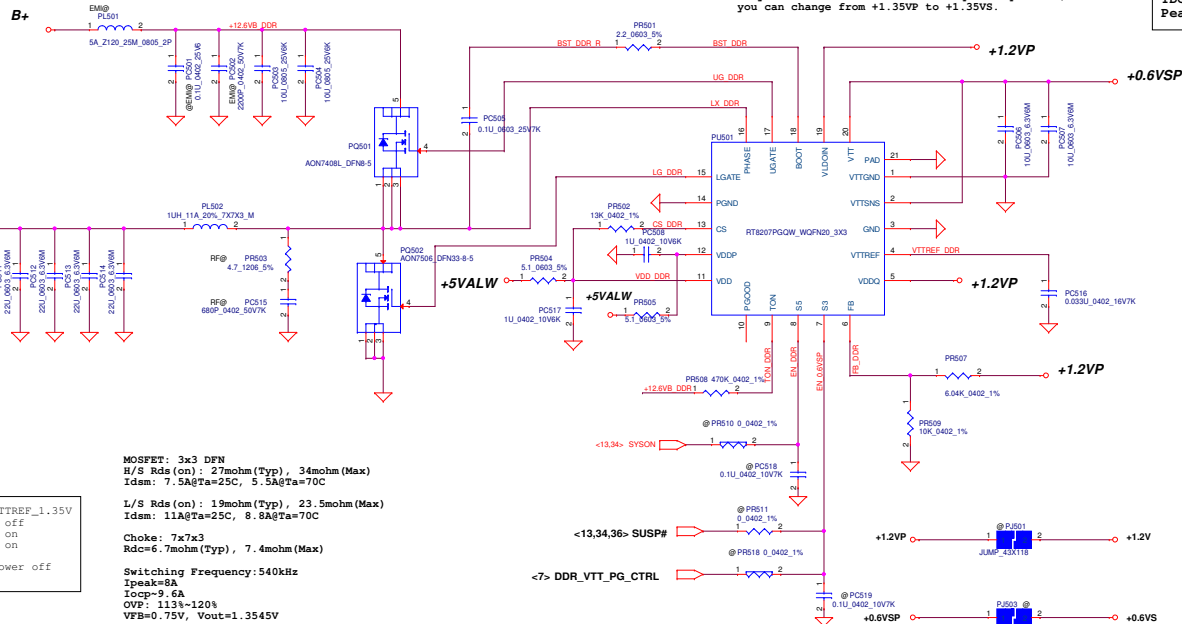


Module model information

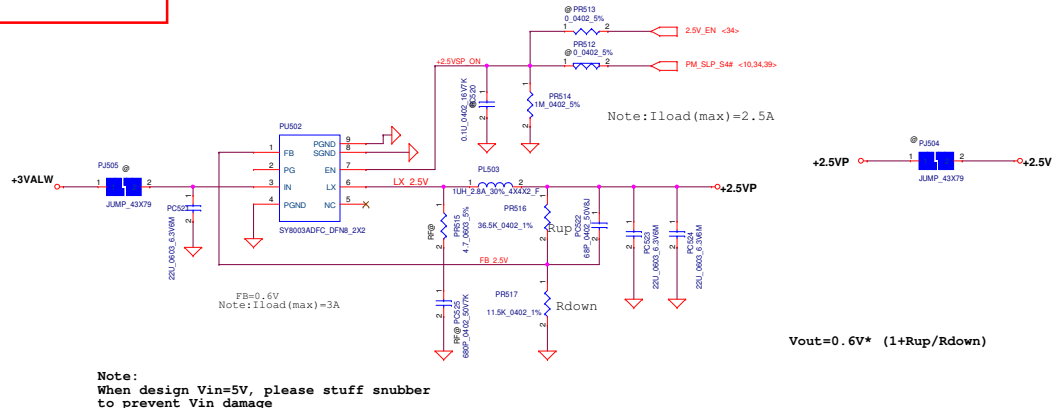
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				Date	Tuesday, June 28, 2016
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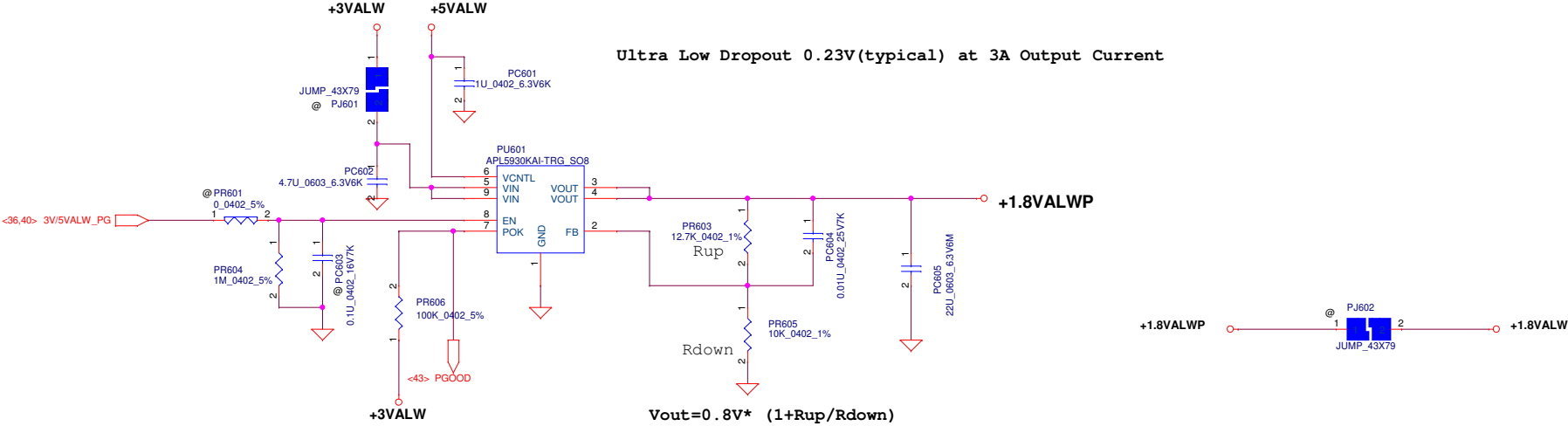
Module model information
SY8003A_V1.mdd



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

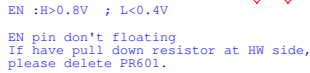
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Issued Date	2015/07/27	Deciphered Date	2016/07/27	Compal Electronics, Inc.	
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Size	Document Number			Rev	
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Date:	Tuesday, June 28, 2016		Sheet	41	of 50

Module model information
APL5930_V2.mdd



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Module model information
SY8288_V1.mdd



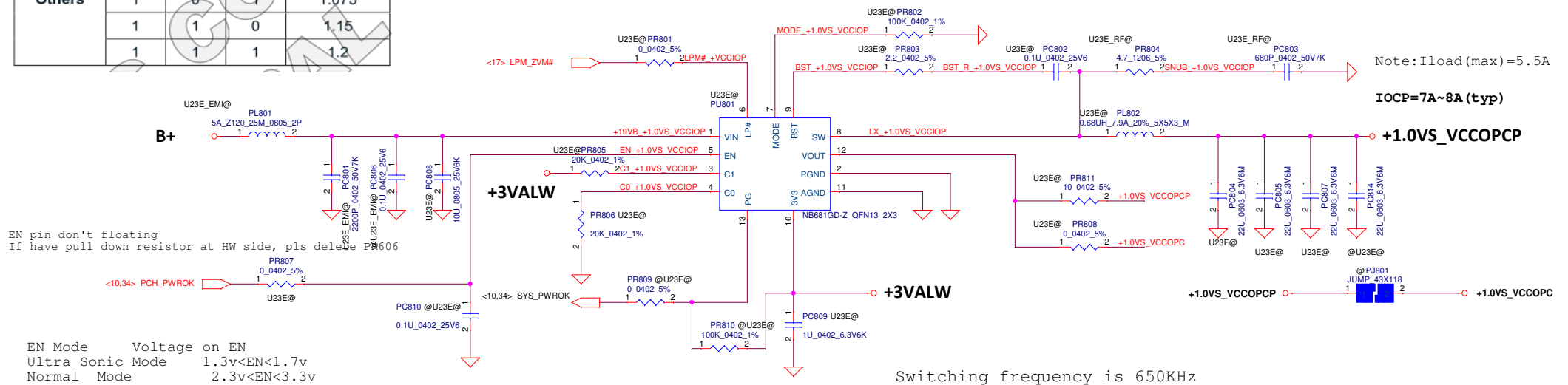
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Issued Date	2015/07/27	Deciphered Date	2016/07/27
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Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

Module model information

NB681_V1.mdd



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CPU CORE

Due to U23e VCC and GTX merged current spec is TBD in PDDG.
Please confirm FAB the setting of PRI23, PRI39 PRI63 for U23e GT and GTX merged.

Module model information

NCP81208_U2223E_COLAY_V1A.mdd for IC portion

NCP81208_U2223E_COLAY_V1B.mdd for SW portion

Copy the schematic to new page,
the co-lay location maybe changed.

RIOUT@GT:
U23e = 22.1K PRI23
U22 = 25.5K PRI23

U23e@ PRI923
22.2K_0402_1%

RPH@GT:
U23e = 130K PRI929, PRI938
U22 = 84.5K PRI929

U23e@ PRI929
110K_0603_1%

For U22:
PRI943=De-pop
For U23e:
PRI943, PRI944=Pop

For U22:
PRI947=2K, PRI954=De-pop
For U23e:
PRI947=2K, PRI954=2K

U22 OCP@GT= 40A
RLIM@GT=12.4K ---->PRI39
U23e OCP@GT= 62A
RLIM@GT=12.4K ---->PRI39
RLIM= IoutLIMIT * Load line/10

U22 IccMAX@GT= 31A
RiccMAX2ph= 49.7K ---->PRI63
U23e IccMAX@GT= 56A
RiccMAX2ph= 87.6k ---->PRI63
RiccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127

U22 Iout@GT= 31A
RIOUT@GT=25.5K ---->PRI23
U23e Iout@GT= 56A
RIOUT@GT=22.1K ---->PRI23
RIOUT= 2* RLIM / (10 * IoutICCMAX * Load line)

U22 Load line@GT= 3.1m
RPH@GT=84.5K ---->PRI30, PRI38
U23e Load line@GT= 2m
RPH@GT=130K ---->PRI30, PRI38

Load line= (RCS2+(RCS1*Rth)/(RCS1+Rth))
* IOUTTOTAL * DCR/RPH

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

NCP81208 Operating Frequency Rosc=24K
I/A and GT are 450KHz and SA is 450KHz

RiccMAX2ph:
U23e@
100K_0402_1%

PSYS:
Please confirm charger pull low resistance.
Charger side should be unpop.

IccMAX@SA= 5A
RiccMAX@SA= 15.8K ---->PRI65
RiccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K ---->PRI14
RIOUTSP= 2V/(gm*(Rth+RCSSP))*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=24K ---->PRI5
RLIMSP= 1.3V/(gm*(Rth+RCSSP))*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.78K ---->PRI4
RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

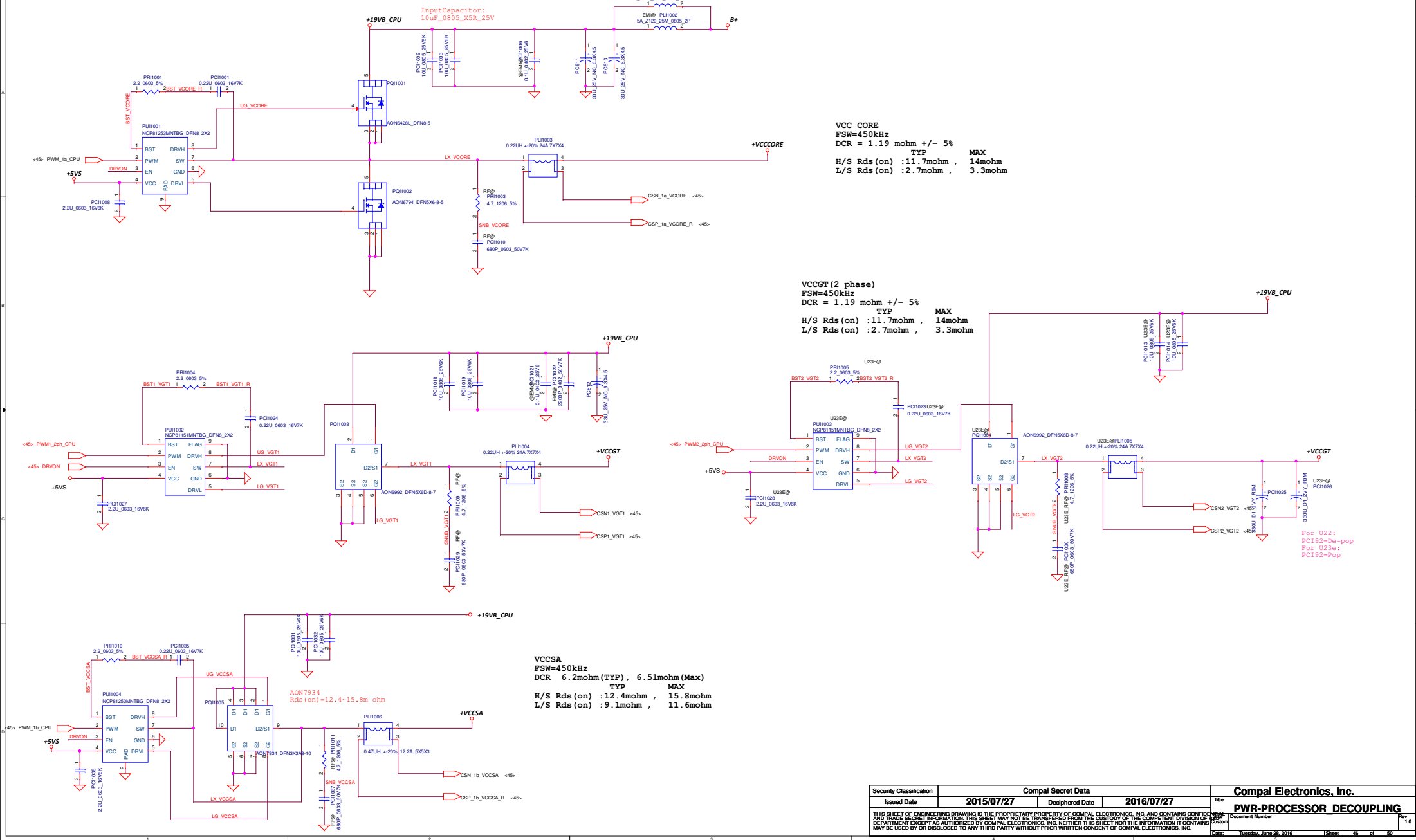
U22 Load line@VCORE= 2.35m
RDRPSP@VCORE=2.1K ---->PRI56
U23e Load line@VCORE= 2.1m
RDRPSP@VCORE=1.87K ---->PRI56
RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 28A
RiccMAX@VCORE= 87.6K ---->PRI64
RiccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=64.9K ---->PRI42
RIOUTSP= 2V/(gm*(Rth+RCSSP))*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@VCORE= 35A
RLIMSP@VCORE=33.4K ---->PRI53
RLIMSP= 1.3V/(gm*(Rth+RCSSP))*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

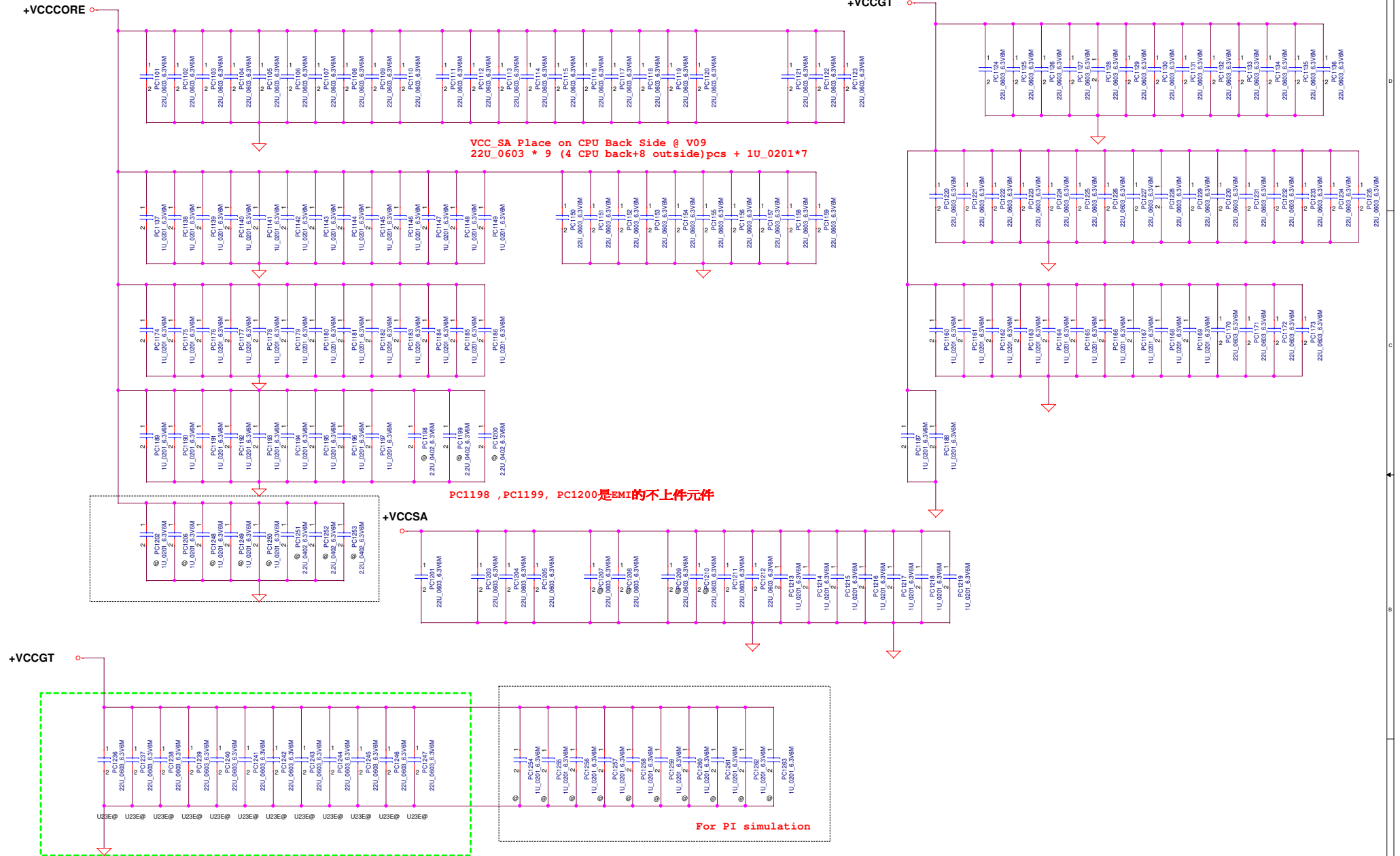
CPU POWER STAGES



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			Date: Tuesday, June 28, 2016
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VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 33 pcs +1U_0201*35 pcs+2.2U_0402*3 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 29 pcs +1U_0201*12 pcs



Module model information
ISL62771_C2_GFX35W_V1A.mdd for IC portion
ISL62771_C2_GFX35W_V1B.mdd for SW portion

VGA_M250=>Link +1.8VGS
VGA_M130=>Link +3VGS

VR_ON
High > 1.6V
Low < 1V

PH1002 near APU_CORE H/S mos
VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1002=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1031=27.4K
100C Assert Threshold: PR1031=16.9K

PH1003 near GFX_CORE choke

PR1058=3.65K, PR1040=2.1K and
PR1046=604 to set loadline -2.1mV/A
while PR1046=594 to set OCP 57.16A
For EDC 45A application.

GFX_core
TDC 30 (1H1L)
Peak Current > 45A
OCP current > 45A
Load line -2.1mV/A
FSW=400kHz
DCR 1.19mohm +/-5%
TYP
H/S Rds(on) :11.7mohm , 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

SH000010N00 (DCR:1.19mohm +/-5%)

+VGA_CORE

+VGA_CORE

+1.5VGS

Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(30.1/20))
Vout=1.503V

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/04	Deciphered Date	2015/01/04	PWR-CPU_CORE/CPU_CORE_NB	
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				1.0	1.0
				LA-E221P	
				Date	Thursday, June 28, 2018
				Sheet	48 of 50

Item	Reason for change	PG#	Modify List	Date	Phase
1	For PI cap un-pop		PC1198, PC1199, PC1200, PC1202, PC1206, PC1248 PC1249, PC1250, PC1251, PC1252, PC1253, PC1254, PC1255, PC1256 PC1257, PC1258, PC1259, PC1260, PC1261, PC1262, PC1263	2016.03.29	SIV
2	change PRI942 to 66.5k ohm		CPU test result	2016.05.13	SIT
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Z BDW	
Date: Tuesday, June 28, 2016				Sheet	49 of 50
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Date	Tuesday, June 28, 2016	Sheet	50	of	50	